AX78140
USB 2.0 to Multi I/O Controller

Features

Document No: AX78140/V1.20/01/17/24

- **Single chip USB 2.0 to Quad Serial Ports and Single Parallel Port controller**

- **USB Device Controller**
  - Integrates on-chip USB 2.0 PHY and controller compliant to USB Spec 2.0 and 1.1
  - Supports all USB 2.0 power saving modes (L1, L2)
  - Supports USB High/Full Speed modes with Bus-power or Self-power device
  - Support USB LPM (Link Power Management)

- **Dual/Quad Serial Port Controller**
  - Two/Four 16c450/16c550 compatible UARTs
  - Supports SIR IrDA mode on any/all ports
  - Supports RS-232, RS-485 and RS-422 serial ports
  - Supports multi-protocol serial transceivers
  - Supports 5, 6, 7, 8 & 9 bit serial data
  - Supports automatic data direction control
  - Supports multi-drop mode with auto address detection
  - Supports hardware and software flow control
  - Supports baud rates from 50bps to 6Mbps
  - Supports custom baud rates from external clock
  - On-Chip 1024-Byte FIFO for upstream and 512-Byte for downstream data transfer for each Serial Port
  - I^2C interface for EEPROM
  - Supports read/write EEPROM through USB interface
  - On-Chip buffers for serial port signals to operate without external transceivers over short cable
  - Pin to Pin compatible with MCS7840
  - Driver backward compatible with MCS7840

- **Support Remote Wake Up Function**
  - Supports Suspend Mode and Remote Wakeup via RXD, RI, DSR, DCD and CTS pin

- **Advanced Power Management Features**
  - Supports USB LPM (Link Power Management)
  - Shut down Transceiver when in Suspend Mode

- **Parallel Port**
  - AX78140 supports optional 2 Serial Port and 1 Parallel Port configuration
  - On-Chip 1024-Byte FIFO for upstream and 512-Byte for downstream data transfer for Parallel Port

- **GPIO**
  - AX78140 supports 1 GPIO pin and 16 optional software controlled GPIO pins
- Integrates on-chip 1.8V and 3.3V voltage regulator and only requires a single 5V power supply
- Single 12MHz clock input from either crystal or oscillator source
- Integrates on-chip power-on reset circuit
- Small form factor with 64-pin LQFP RoHS compliant package
- Operating temperature range: -40°C to +85°C

- **Applications**
  - Serial Attached Devices
  - Modems, Generic Serial Devices
  - Serial-Port Server
  - Data Acquisition System
  - POS Terminal & Industrial PC

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Typical System Block Diagrams

- **Hosted by USB to operate with Quad Serial Ports**

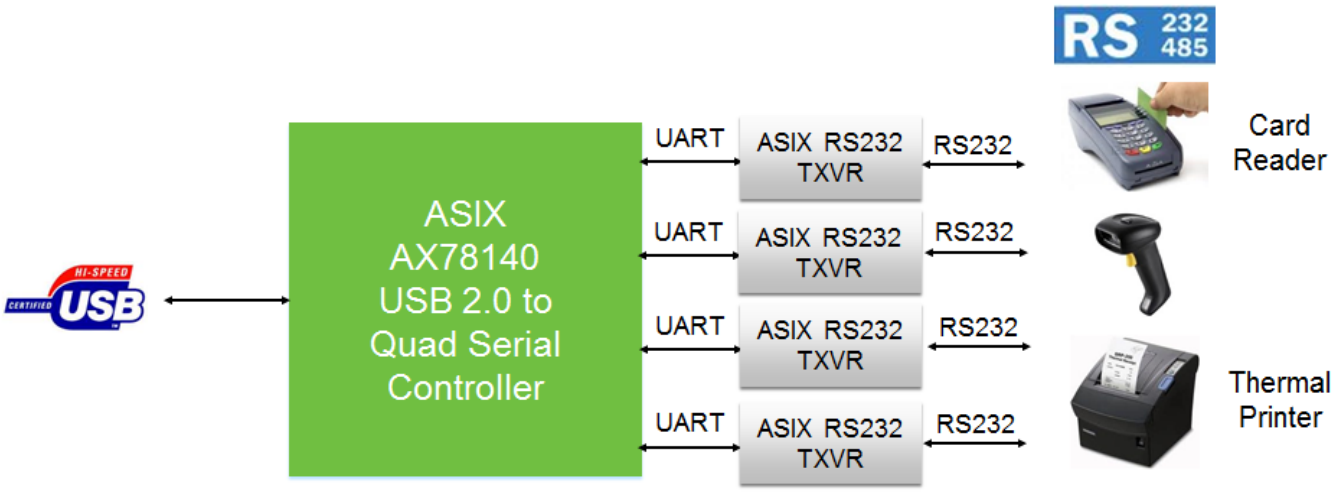

Figure 1: USB 2.0 to quad serial ports

- **Hosted by USB to operate with Dual Serial Ports and Single Parallel Port**

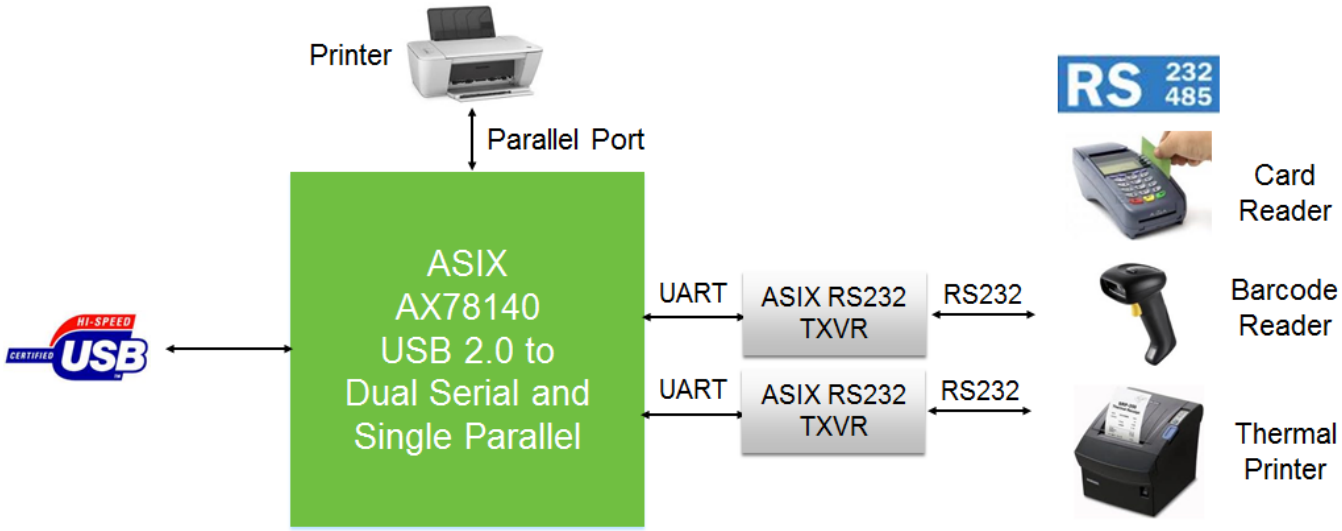

Figure 2: USB 2.0 to dual serial ports and single parallel port

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1 Introduction

1.1 General Description

With the rapid proliferation of USB interface in the embedded world, developers are looking for easiest ways to add USB to microcontroller-based applications in their design. ASIX's new AX78140 features three USB connectivity bridge solutions including USB 2.0 to Quad Serial Ports and USB 2.0 to Dual Serial Ports and Single Parallel Port controllers. For enabling smooth migration from legacy system using ASIX's MCS7840, AX78140 provides pin-to-pin compatible and driver backward compatible with MCS7840.

AX78140 is a USB 2.0 to Quad Serial Ports and Single Parallel Port controller. It has been developed to connect a wide range of standard serial devices to a USB host.

The AX78140 supports the following serial communication programs including: HyperTerminal, PComm, Windows direct connection, Windows dial-up connection through modem, Networking over IrDA and Windows direct connection over IrDA, and Minicom.

The AX78140, in 64-pin LQFP, is available with RoHS compliant package and supports industrial temperature range from -40 to 85°C.

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1.2 Block Diagram

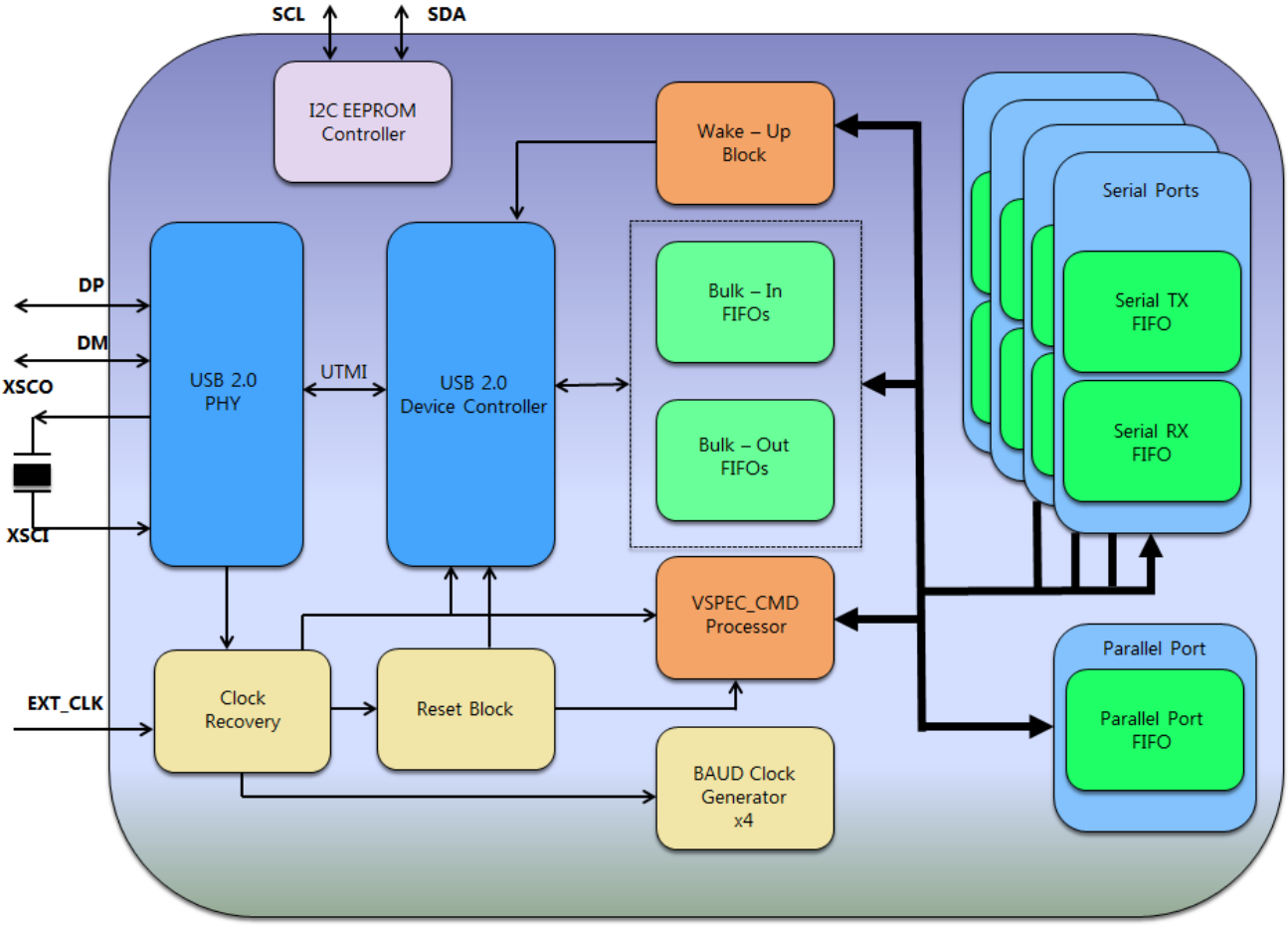

Figure 3: Block Diagram

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1.3 Pinout Diagram

- 64-pin LQFP package

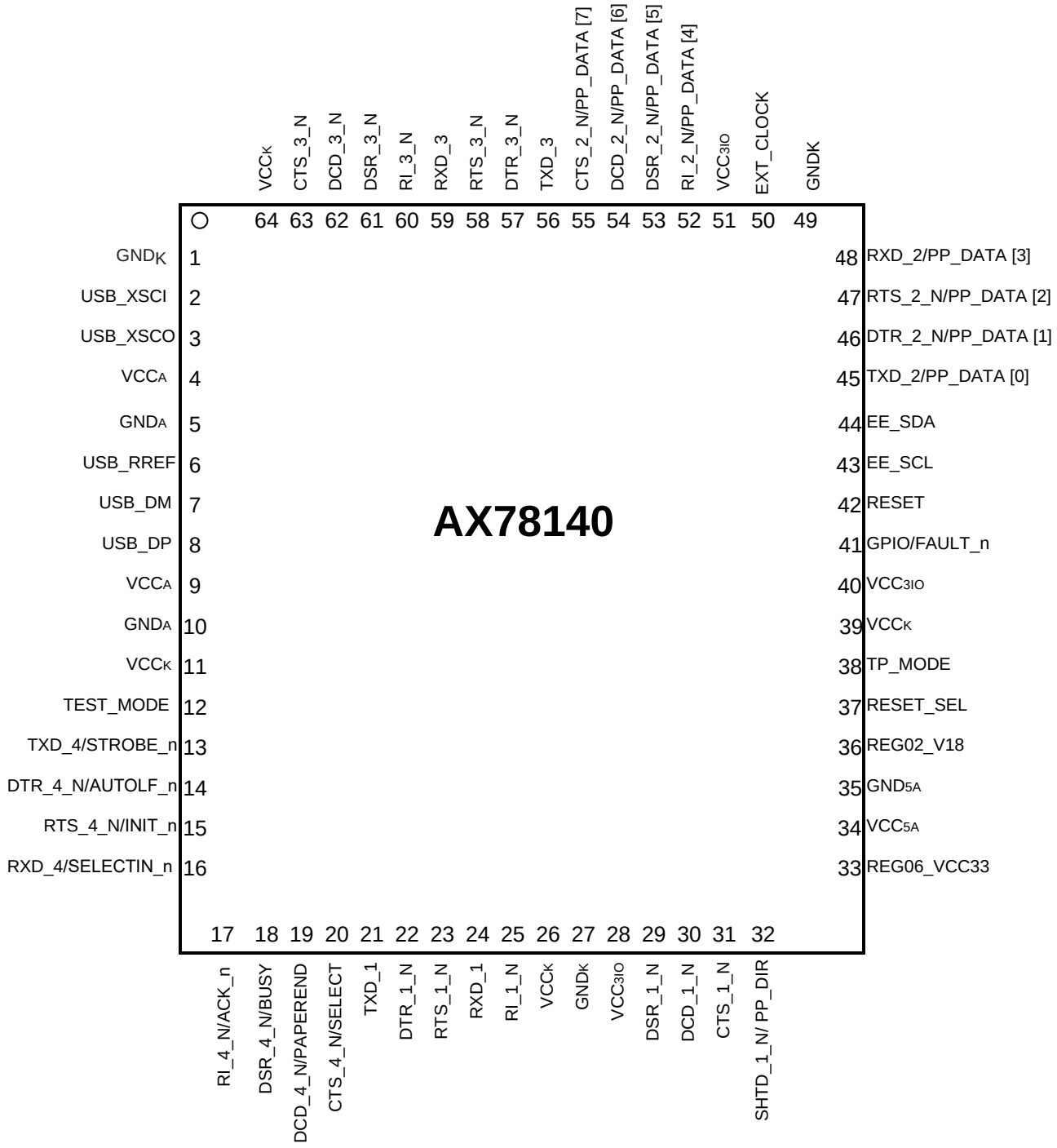

Figure 4: Pinout Diagram

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2 Signal Description

The following abbreviations apply to the following pin description table.

I18	**Input, 1.8V**	**AI**	**Analog Input**
I3	**Input, 3.3V**	**AO**	**Analog Output**
I5	**Input, 3.3V with 5V tolerant**	**AB**	**Analog Bi-directional I/O**
O5	**Output, 3.3V with 5V tolerant**	**PU**	**Internal Pull Up (75K ohm)**
B5	**Bi-directional I/O, 3.3V with 5V tolerant**	**PD**	**Internal Pull Down (75K ohm)**
B3	**Bi-directional I/O, 3.3V**	**S**	**Schmitt Trigger**
P	**Power/GND**	**T**	**Tri-stateable**

2.1 64-pin Pinout Description

Pin Name	Type	Pin No	Pin Description
USB Interface			
USB_DM	AB	7	USB 2.0 data negative pin.
USB_DP	AB	8	USB 2.0 data positive pin.
Clock Pins			
USB_XSCI	I3	2	12Mhz crystal or oscillator clock input.
USB_XSCO	O3	3	12Mhz crystal or oscillator clock output.
Serial EEPROM Interface			
EE_SCL	B5/PU/T	43	2-Wire(I^2C) EEPROM Clock. Default=High(1)
EE_SDA	B5/PU/T	44	2-Wire(I^2C) EEPROM Data in/out. Default=High(1)
Misc. Pins			
USB_RREF	I5/PU/S	6	External Reference Resistor (12.1 KΩ, 1%) Connect resistor to Analog GND.
TEST_MODE	I5/PD/S	12	Test Mode Pin, (active high). Default = Low (0) When TEST_MODE = 1, PLL, Core, and SCAN/BIST/ Memory BIST testing can be performed. Set TEST_MODE = 0 for normal operation.
TXD_4/ STROBE_n	B5/S	13	Serial Port 4 Transmit Data out to transceiver or IrDA data out to IR LED. If AX78140 is configured in 2S1P mode, this pin will operate as STROBE_n.
DTR_4_N/ AUTOLF_n	B5/S	14	Serial Port 4 Data Terminal Ready (in serial protocol), active low. If AX78140 is configured in 2S1P mode, this pin will operate as AUTOLF_n.
RTS_4_N/ INIT_n	B5/S	15	Serial Port 4 Request To Send (in serial protocol), active low. If AX78140 is configured in 2S1P mode, this pin will operate as INIT_n.
RXD_4/ SELECTIN_n	B5/S	16	Serial Port 4 Serial Receive Data in from transceiver or IrDA data in from IrDA detector. If AX78140 is configured in 2S1P mode, this pin will operate as SELECTIN_n.
RI_4_N/ ACK_n	B5/S	17	Serial Port 4 Ring Indicator, active low. If AX78140 is configured in 2S1P mode, this pin will operate as ACK_n. This pin can also perform as a SW controlled GPIO.
DSR_4_N/ BUSY	B5/S	18	Serial Port 4 Data Set Ready (in serial protocol), active low. If AX78140 is configured in 2S1P mode, this pin will operate as BUSY. This pin can also perform as a SW controlled GPIO.
DCD_4_N/ PAPEREND	B5/S	19	Serial Port 4 Data Carrier Detect (in serial protocol), active low. If AX78140 is configured in 2S1P mode, this pin will operate as PAPEREND. This pin can also perform as a SW controlled GPIO.
CTS_4_N/ SELECT	B5/S	20	Serial Port 4 Clear To Send (in serial protocol), active low. If AX78140 is configured in 2S1P mode, this pin will operate as SELECT. This pin can also perform as a SW controlled GPIO.

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TXD_1	B5/S	21	Serial Port 1 Transmit Data out to transceiver, or IrDA data out to IR LED.
DTR_1_N	O5	22	Serial Port 1 Data Terminal Ready (in serial protocol), active low.
RTS_1_N	O5	23	Serial Port 1 Request To Send (in serial protocol), active low.
RXD_1	I5/S	24	Serial Port 1 Serial Receive Data in from transceiver, or IrDA data in from IrDA detector.
RI_1_N	B5/S	25	Serial Port 1 Ring Indicator, active low. This pin can also perform as a SW controlled GPIO.
DSR_1_N	B5/S	29	Serial Port 1 Data Set Ready (in serial protocol), active low. This pin can also perform as a SW controlled GPIO.
DCD_1_N	B5/S	30	Serial Port 1 Data Carrier Detect (in serial protocol), active low. This pin can also perform as a SW controlled GPIO.
CTS_1_N	B5/S	31	Serial Port 1 Clear To Send (in serial protocol), active low. This pin can also perform as a SW controlled GPIO.
SHTD_1_N/ PP_DIR	B5/S	32	Shut Down External Serial Transceiver during normal operation, active low by default, can be configured active high by using DCR setting. If AX78140 is configured in 2S1P mode, this pin will operate as PP_DIR
RESET_SEL	I18/S	37	Select the polarity of RESET signal. Please refer to **2.2 Hardware Setting For Operation Mode.**
TP_MODE	I3/PD/S	38	For internal test purpose, so always tie to GND.
GPIO/ FAULT_n	B5/S	41	GPIO/USB Max. Power GPIO_MODE - Bidirectional GPIO bit. The direction (Input or Output) is controlled by the DCR for Serial Port #1. This pin is also used to indicate the USB Max. Power configuration while reporting USB device configuration descriptor to USB host. (High = 500mA; Low = 100mA) If AX78140 is configured in 2S1P mode, this pin will operate as FAULT_n.
RESET	I5/S	42	Reset signal. The polarity is determined by RESET_SEL pin.
TXD_2/ PP_DATA [0]	B5/S	45	Serial Port 2 Transmit Data out to transceiver, or IrDA data out to IR LED. If AX78140 is configured in 2S1P mode, this pin will operate as PP_DATA [0].
DTR_2_N/ PP_DATA [1]	B5/S	46	Serial Port 2 Data Terminal Ready (in serial protocol), active low. If AX78140 is configured in 2S1P mode, this pin will operate as PP_DATA [1].
RTS_2_N/ PP_DATA [2]	B5/S	47	Serial Port 2 Request To Send (in serial protocol), active low. If AX78140 is configured in 2S1P mode, this pin will operate as PP_DATA [2].
RXD_2/ PP_DATA [3]	B5/S	48	Serial Port 2 Serial Receive Data in from transceiver or IrDA data in from IrDA detector. If AX78140 is configured in 2S1P mode, this pin will operate as PP_DATA [3].
EXT_CLOCK	I5/S	50	Input Clock from external world. In normal operation mode, clock can be supplied to serial ports and used for custom BAUD Rate of user's choice. In test mode, clock will be the test clock input from external world.
RI_2_N/ PP_DATA [4]	B5/S	52	Serial Port 2 Ring Indicator, active low. If AX78140 is configured in 2S1P mode, this pin will operate as PP_DATA [4]. This pin can also perform as a SW controlled GPIO.
DSR_2_N/ PP_DATA [5]	B5/S	53	Serial Port 2 Data Set Ready (in serial protocol), active low. If AX78140 is configured in 2S1P mode, this pin will operate as PP_DATA [5]. This pin can also perform as a SW controlled GPIO.
DCD_2_N/ PP_DATA [6]	B5/S	54	Serial Port 2 Data Carrier Detect (in serial protocol), active low. If AX78140 is configured in 2S1P mode, this pin will operate as PP_DATA [6]. This pin can also perform as a SW controlled GPIO.
CTS_2_N/ PP_DATA [7]	B5/S	55	Serial Port 2 Clear To Send (in serial protocol), active low. If AX78140 is configured in 2S1P mode, this pin will operate as PP_DATA [7]. This pin can also perform as a SW controlled GPIO.

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TXD_3	O5	56	Serial Port 3 Transmit Data out to transceiver, or IrDA data out to IR LED.
DTR_3_N	B5/S	57	Serial Port 3 Data Terminal Ready (in serial protocol), active low.
RTS_3_N	B5/S	58	Serial Port 3 Request To Send (in serial protocol), active low.
RXD_3	I5/S	59	Serial Port 3 Serial Receive Data in from transceiver, or IrDA data in from IrDA detector.
RI_3_N	B5/S	60	Serial Port 3 Ring Indicator, active low. This pin can also perform as a SW controlled GPIO.
DSR_3_N	B5/S	61	Serial Port 3 Data Set Ready (in serial protocol), active low. This pin can also perform as a SW controlled GPIO.
DCD_3_N	B5/S	62	Serial Port 3 Data Carrier Detect (in serial protocol), active low. This pin can also perform as a SW controlled GPIO.
CTS_3_N	B5/S	63	Serial Port 3 Clear To Send (in serial protocol), active low. This pin can also perform as a SW controlled GPIO.
Power and Ground Pins			
VCC_K	P	11, 26, 39, 64	Digital Core Power. 1.8V.
VCC_A	P	4, 9	Analog Power for USB transceiver. 3.3V.
GND_A	P	5, 10	Analog Ground for USB transceiver.
GND_K	P	1,27, 49	Digital Ground
VCC_{3IO}	P	28, 40, 51	Digital I/O Power. 3.3V.
REG06_VCC33	P	33	3.3V output from internal regulator.
VCC_{5A}	P	34	5V power input to internal regulator.
GND_{5A}	P	35	Ground for 5V input.
REG02_V18	P	36	1.8V output from internal regulator.

Table 2: Pinout Description

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2.2 Hardware Setting For Operation Mode

GPIO is a general purpose I/O normally controlled by vendor commands. Users can change this pin to change the max power 100mA or 500mA

- GPIO pin: Determines whether descripter will report max power 100mA or 500mA

GPIO	Description
0	Descripter report max power 100mA. Please connect GND with a pulled-down resistor (4.7Kohm).
1	Descripter report max power 500mA. Please connect VCC with a pulled-up resistor (4.7Kohm).

- RESET_SEL pin: Determines the polarity of RESET.

RESET_SEL	Description
0	RESET pin active low. Please connect GND with a pulled-down resistor (4.7Kohm).
1	RESET pin active high. Please connect VCC with a pulled-up resistor (4.7Kohm).

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3 Function Description

3.1 Internal Regulators

An internal two rail DC-DC Regulator is provided to convert 5V to 1.8V for Core Logic and convert the 5V input to 3.3V for I/O functions. These regulators eliminate the need for external voltage sources.

3.2 USB 2.0 PHY

This is the physical layer of the USB interface. The USB2.0 PHY communicates with the USB2.0 Device Controller logic through a UTMI interface to send/receive data on the USB bus.

3.3 USB 2.0 Device Controller

The USB2.0 Device Controller interfaces to the internal bridge and communicates with the serial ports through the bridge logic. The device controller logic is connected to a physical layer USB2.0 PHY which provides the USB bus interface for the chip. The device controller responds to standard as well as vendor specific requests from USB2.0 and USB1.1 Hosts.

3.4 Bridge

The bridge logic, including Bulk-In and Bulk-Out FIFOs, controls traffic between the USB 2.0 device controller and the serial port controllers. The bridge logic has synchronous RAM memories with ping- pong FIFO control logic to buffer data in either direction (Bulk-In and Bulk-Out) and send it to the other side without loss. Control logic prevents overflow or underflow conditions in the memory.

The Bridge also includes Interrupt-In endpoint controller which gives the status of the serial port interrupt registers to the USB2.0 Device Controller. The USB host controller periodically polls the interrupt endpoint and reads the status of the interrupts.

3.5 Vendor Command Processor

The bridge logic interfaces to a Vendor Specific Command Processor (VSPEC_CMD_Processor) block containing commands/register settings (BAUD settings etc.) which are specific to this device.

3.6 Serial Port Controllers

The Serial Port Controllers are linked to the bridge and send/receive data from the bridge interface. Each serial port controller has register logic controlling BAUD rates (50 bps ~ 6 Mbps), stop-bits, and parity bit settings. Each serial port has synchronous RAM memories acting as transmit and receive FIFOs to buffer outgoing and incoming data. This block has registers for interrupts, line status, and line control features which can be accessed by software. The Serial Port Controllers can interface to external RS-232 / RS-422 / RS-485 transceivers.

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3.7 Parallel Port Controller

The Parallel Port Controller is linked to the bridge and send/receive data from the bridge interface. It has register logic and synchronous RAM memories acting as transmit and receive FIFOs to buffer outgoing and incoming data. This block has registers for interrupts, data, and control features which can be accessed by software.
When AX78140 is configured to 2S1P mode, this Parallel Port Controller will be enabled to work.

3.8 Wake-Up Block

The Wakeup block is used for remote wakeup control. The USB host can suspend operation of the device. The remote wakeup block checks for activity on the serial port pins, and if information is available, it issues a remote wakeup request to the USB2.0 Device Controller. The Device Controller in turn requests a remote wakeup to the external host. The host issues the "Resume Signaling" command to the device, which then resumes normal operation.

3.9 I^2C EEPROM Controller

AX78140 can use the I^2C Hardware Configuration EEPROM (HWCFGEE) to overwrite some hardware default values during boot up and retrieves information necessary for serial port settings, Product-IDs, Vendor-IDs and other control information if the Configuration EEPROM existed and the checksum is correct. If EEPROM does not exist or its checksum is incorrected, Hardware will skip to load the content or give up the loaded values from EEPROM then still use the hardware default values in each chip mode for the chip operation. It uses a serial EEPROM with I^2C interface with at least 256x8 (2048 bits), for example Atmel AT24C02. The 7-bit device address of the I^2C Hardware Configuration EEPROM on application circuit must be set to 1010000b. Note that the Hardware will only use the "8-bit Device Memory Address Format" to load HWCFGEE when boot up.

3.10 Clock Generation and Reset

The Clock Generation logic is used to generate the clocks for the various BAUD rates supported by the device. The Resets block has logic for synchronous de-assertion and asynchronous assertion of Resets in the respective clock domains to various blocks.

3.11 BAUD Clock Generators

The BAUD Clock Generator block generates clocks for each of the Serial Port Controllers depending on the BAUD settings from the host. A source clock is generated from the Clock Recovery block which is further divided or used as is by the BAUD Clock Generator logic depending on the BAUD settings.

3.12 GPIO

The GPIO pin (pin #41) is a general purpose I/O normally controlled by vendor commands. Note that this pin is also for USB Max. Power hardware configuration (Section 2-2). Please make sure the GPIO pin setting won't affect the USB Max. Power hardware configuration during hardware reset.

AX78140 can also support extra 16 optional software controller GPIO pins (pin #17~20, 25, 29~31, 52~55, 60~63) if users need not use the RI/DSR/DCD/CTS signals of Serial Port 1~4.

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4 I²C EEPROM Memory Map

Offset	# of Bytes	Name	Description
0x01~0x00	2	EE Check	EEPROM Present Check value = 0x9710
0x03~0x02	2	VID	Vendor ID = 0x9710
0x05~0x04	2	PID	Product ID = 0x7840
0x07~0x06	2	RN	Release Number in BCD format = 0x0001
0x08	1	SER1_DCR0	Device Configuration Registers (SER1_DCR0)
0x09	1	SER1_DCR1	Device Configuration Registers (SER1_DCR1)
0x 0A	1	SER1_DCR2	Device Configuration Registers (SER1_DCR2)
0x 0B	1	SER2_DCR0	Device Configuration Registers (SER2_DCR0)
0x 0C	1	SER2_DCR1	Device Configuration Registers (SER2_DCR1)
0x 0D	1	SER2_DCR2	Device Configuration Registers (SER2_DCR2)
0x 0E	1	SER3_DCR0	Device Configuration Registers (SER3_DCR0)
0x 0F	1	SER3_DCR1	Device Configuration Registers (SER3_DCR1)
0x 10	1	SER3_DCR2	Device Configuration Registers (SER3_DCR2)
0x 11	1	SER4_DCR0	Device Configuration Registers (SER4_DCR0)
0x 12	1	SER4_DCR1	Device Configuration Registers (SER4_DCR1)
0x 13	1	SER4_DCR2	Device Configuration Registers (SER4_DCR2)
0x 14	1	intr_pg_fs	Binterval value for Full Speed
0x 15	1	intr_pg_hs	Binterval value for High Speed
0x17~0x16	2	Language ID	Language ID in HEX Format (0x0409 default)
0x47~0x18	48	Manufacture ID	“MosChip Semiconductor” in UNICODE
0x71~0x48	42	Product Name	“USB-Serial Controller” in UNICODE
0x81~0x72	16	Serial Number	“X7X6X5X4X3X2X1X0” in UNICODE
0x82	1	Check Sum	Check Sum field
0x86~0x83	4	BOS Descriptor	bmAttribute: 0x0000_F11E
0x87	1	bcdUSB LB	USB Specification Release Number (0x01)
0x88	1	LPM L1 Ctrl Reg	LPM L1 control Register (0x03)
0x89	1	bMaxPower	Configuration Descriptor bMaxPower (0xFA)
0x8A	1	bIClass	Configuration Descriptor bIClass (0xFF)
0x8B	1	bISubClass	Configuration Descriptor bISubClass (0x00)
0x8C	1	bIProto	Configuration Descriptor bIProto (0xFF)
0x8D	1	bClass	Device Descriptor bClass (0xFF)
0x8E	1	bSubClass	Device Descriptor bSubClass (0x00)
0x8F	1	bProto	Device Descriptor bProto (0xFF)
0x90	1	PP_ENA	Enable Printer Port function

Table 2: Serial EEPROM Memory Map

Note_1: The value of EEPROM Checksum field located at EEPROM offset 0x82. The correct value must be equal to (0xFF - SUM [EEPROM offset 0x83~0x90]).

Note_2: Total usage is about 145 bytes.

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4.1 Detailed Description

The following sections provide detailed descriptions for some of the fields in memory maps of I^2C EEPROM

4.1.1 Serial Port 1 – Device Configuration Register 0 (0x08)

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Reserved	IrDA_Mode	RTS_ CM		GPIO_ Mode		Reserved	RS_ SDM

DCR0 Bit	Name	Definition	Default Value
0	RS_SDM	**RS-232 / RS-422 / RS-485 Transceiver Shut-Down Mode:** 0: Do not shut down the transceiver even when USB SUSPEND is engaged 1: Shut down the transceiver when USB SUSPEND is engaged	1
1	Reserved	Reserved	0
[3:2]	GPIO_ Mode	GPIO direction mode: 00: GPIO = Input 10: GPIO = Output 01, 11: Reserved	00
[5:4]	RTS_CM	**RTSM RTS Control Method:** 00: RTS is controlled by Control Bit Map. Signal is active low; 01: RTS is controlled by Control Bit Map. Signal is active high; 10: Drive RTS active When Downstream Data Buffer is NOT EMPTY; Otherwise Drive RTS inactive. 11: Drive RTS inactive When Downstream Data Buffer is NOT EMPTY; Otherwise Drive RTS active.	00
6	IrDA_Mode	IrDA Mode: 0: RS-232 / RS-422 / RS-485 Serial Port Mode. 1: IrDA Mode.	0
7	Reserved	Reserved	0

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4.1.2 Serial Port 1 – Device Configuration Register 1 (0x09)

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Reserved	Interrupt IN Endpoint Status	PLL_ Power-Down Bypass Control	RW_ INHB	Tx_I_ PMG		GPIO_I_ PMG	

DCR1 Bit	Name	Definition	Default Value
[1:0]	GPIO_I_ PMG	**These two bits set the output current of the GPIO lines:** 00: 6mA 01:8 mA (Default) 10:10 mA 11:12 mA	01
[3:2]	Tx_I_ PMG	**These two bits set the output current of Serial output signals TxD, DTR_n and RTS_n:** 00: 6 mA 01: 8 mA (Default) 10: 10 mA 11: 12 mA	01
4	RW_ INHB	**RW_INH Remote Wake Inhibit:** 0: Enable the USB Remote Wakeup function 1: Inhibit the USB Remote Wakeup function	0
5	PLL_ Power-Down Bypass Control	**PLL Power Down Bypass Control:** 0: Enables PLL Power-Down 1: Disables PLL Power-Down	0
6	Interrupt IN Endpoint Status	**Interrupt IN Endpoint Status:** 0: Interrupt Endpoint returns 5 Bytes of data. 1: Interrupt Endpoint returns 5 Bytes + 8 Bytes of the Bulk-In/Out memory controller status	0
7	Reserved	Reserved	1

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4.1.3 Serial Port 1 – Device Configuration Register 2 (0x0A)

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
SHDN_ POL	Reserved	RWU_ Mode	EWU_ Rx	EWU_ DSR	EWU_ RI	EWU_ DCD	EWU_ CTS

DCR2 Bit	Name	Definitio n	Default Value
0	EWU_ CTS	**Enable Wake Up Trigger on CTS:** 0: Disabled. 1: Enable Wake Up Trigger on CTS State Changes.	0
1	EWU_ DCD	**Enable Wake Up Trigger on DCD:** 0: Disabled 1: Enable Wake Up Trigger on DCD State Changes.	0
2	EWU_ RI	**Enable Wake Up Trigger on RI:** 0: Disabled 1: Enable Wake Up Trigger on RI State Changes.	1
3	EWU_ DSR	**Enable Wake Up Trigger on DSR:** 0: Disabled 1: Enable Wake Up Trigger on DSR State Changes.	0
4	EWU_ Rx	**Enable Wake Up Trigger on RXD:** 0: Disabled 1: Enable Wake Up Trigger on RXD State Changes.	0
5	RWU_ Mode	**Remote Wakeup Mode:** 0: Disabled 1: Engages Remote Wakeup, The device issues Resume Signal.	1
6	Reserved	Reserved	0
7	SHDN_ POL	**SHDN Polarity:** 0: Pin 12 Active Low Shut-Down Signal. 1: Pin 12 Active High Shut-Down Signal.	0

Note: Wake up defined above can work only when DCR0[6] = 0 and DCR1[4] = 0.

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4.1.4 Serial Port (2, 3, & 4) – Device Configuration Register 0 (0x0B, 0x0E, 0x11)

The Configuration Registers for these three Serial Ports are all identical.
They are very similar to Serial Port 1, but have a few less configuration options.

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Reserved	IrDA_ Mode	RTS_ CM		Reserved			RS_ SDM

DCR0 Bit	Name	Definition	Default Value
0	RS_ SDM	**RS-232 / RS-422 / RS-485 Transceiver Shut-Down Mode:** 0:Do not shut down the transceiver even when USB SUSPEND is engaged 1: Shut down the transceiver when USB SUSPEND is engaged	1
[3:1]	Reserved	Reserved	000
[5:4]	RTS_ CM	**RTSM RTS Control Method:** 00: RTS is controlled by Control Bit Map. Signal is active low; 01: RTS is controlled by Control Bit Map. Signal is active high; 10: Drive RTS active when Downstream Data Buffer is NOT EMPTY; Otherwise Drive RTS inactive. 11: Drive RTS inactive when Downstream Data Buffer is NOT EMPTY; Otherwise Drive RTS active.	00
6	IrDA_ Mode	**IrDA Mode:** 0: RS-232 / RS-422 / RS-485 Serial Port Mode. 1: IrDA Mode.	0
7	Reserved	Reserved	0

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4.1.5 Serial Port (2, 3, & 4) – Device Configuration Register 1 (0x0C, 0x0F, 0x12)

The Configuration Registers for these three Serial Ports are all identical with reserved.

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Reserved							

DCR1 Bit	Name	Definition	Default Value
[7:0]	Reserved	Reserved	0x80

4.1.6 Serial Port (2, 3, & 4) – Device Configuration Register 2 (0x0D, 0x10, 0x13)

The Configuration Registers for these three Serial Ports are all identical.
They are very similar to Serial Port 1, but have a few less configuration options.

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Reserved	Reserved	RWU_ Mode	EWU_ Rx	EWU_ DSR	EWU_ RI	EWU_ DCD	EWU_ CTS

DCR2 Bit	Name	Definition	Default Value
0	EWU_ CTS	**Enable Wake Up Trigger on CTS:** 0: Disabled 1: Enable Wake Up Trigger on CTS State Changes.	0
1	EWU_ DCD	**Enable Wake Up Trigger on DCD:** 0: Disabled 1: Enable Wake Up Trigger on DCD State Changes.	0
2	EWU_ RI	**Enable Wake Up Trigger on RI:** 0: Disabled 1: Enable Wake Up Trigger on RI State Changes.	1
3	EWU_ DSR	**Enable Wake Up Trigger on DSR:** 0: Disabled 1: Enable Wake Up Trigger on DSR State Changes.	0
4	EWU_ Rx	**Enable Wake Up Trigger on RXD:** 0: Disabled 1: Enable Wake Up Trigger on RXD State Changes.	0
5	RWU_ Mode	**Remote Wakeup Mode:** 0: Disabled 1: Engages remote wakeup. The Device issues resume signal.	1
6	Reserved	Reserved	0
7	Reserved	Reserved	0

Note: Wake up defined above can work only when DCR0[6] = 0 and DCR1[4] = 0.

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4.1.7 LPM_L1_CTRL_REG (0x88)

The Control Register for LPM L1 function.

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Reserved				lpm_rej	rsm_by_no_ idle	chk_besl	lpm_rcv_ena

LLCR Bit	Name	Definition	Default Value
0	Lpm_rcv_ena	**LPM receive enable:** 0: Disabled 1: Enable receiving of EXT packet of LPM transaction.	1
1	Chk_besl	**Check BESL:** 0: Disabled 1: Check BESL value of LPM transaction	1
2	rsm_by_no_ idle	**Resumed by non-idle signaling:** 0: Disabled 1: Device is resumed by non-idle signaling in L1 (sleep) state	0
3	lpm_rej	**LPM request:** 0: Disabled 1: Device always reject LPM request.	0
[7:4]	Reserved	Reserved	0000

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4.1.8 PP_EN_REG (0x90)

The Configuration Register for enabling Parallel Port Confinguration.

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Reserved						SELF_PWR	PP_EN

PPER Bit	Name	Deinition	Default Value
0	PP_EN	**Parallel printer port enable:** 0: Parallel printer port is disabled 1: Parallel printer port is enabled.	0
1	SELF_PWR	**Self-powered setting&enable:** 0: Self-powered = 1'b0 1: Self-powered = 1'b1	0
[7:2]	Reserved	Reserved	0000000

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4.1.9 USB Descriptor Registers (0x83~0x87, 0x89~0x8F)

These registers are setting and mapping to Device/Configuration Descriptors of USB2.0 spec, Chapter 9 USB Device Framework. And, they are almost fixed for no change except offset 0x89, bMaxPower.

The offset 0x89, bMaxPower is used to configure the "bMaxPower" field of Standard Configuration Descriptor that will be reported to the USB host controller when the GET_DESCRIPTOR command with CONFIGURATION type is issued. Please refer to below table or "Section 9.6.3 Configuration" of Universal Serial Bus 2.0 Spec for the detailed description of the "bMaxPower" field of Standard Configuration Descriptor. This field is used to define the Maximum power consumption of the USB device drawn from the USB bus in this specific configuration.

The default value of Bus Power is 0xFA: the power value is 500mA (Unit = 2mA). For Self Power device, you may set 0x32: the power value is 100mA (Unit = 2mA)

Offset	Field	Size	Value	Description
8	*bMaxPower*	1	mA	Maximum power consumption of the USB device from the bus in this specific configuration when the device is fully operational. Expressed in 2 mA units (i.e., 50 = 100 mA). Note: A device configuration reports whether the configuration is bus-powered or self-powered. Device status reports whether the device is currently self-powered. If a device is disconnected from its external power source, it updates device status to indicate that it is no longer self-powered. A device may not increase its power draw from the bus, when it loses its external power source, beyond the amount reported by its configuration. If a device can continue to operate when disconnected from its external power source, it continues to do so. If the device cannot continue to operate, it fails operations it can no longer support. The USB System Software may determine the cause of the failure by checking the status and noting the loss of the device's power source.

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5 USB Configuration Structure

5.1 USB Configuration

The AX78140 supports 1 Configuration.

5.2 USB Interface

The AX78140 supports 1 interface.

5.3 USB Endpoints

The AX78140 supports following 10 endpoints:

- Endpoint 0: Control endpoint. It is used for configuring the device.
- Endpoint 1: Serial port 1 bulk-in.
- Endpoint 2: Serial port 1 bulk-out.
- Endpoint 3: Serial port 2 or parallel port bulk-in.
- Endpoint 4: Serial port 2 or parallel port bulk-out.
- Endpoint 5: Serial port 3 bulk-in.
- Endpoint 6: Serial port 3 bulk-out.
- Endpoint 7: Serial port 4 bulk-in
- Endpoint 8: Serial port 4 bulk-out.
- Endpoint 9: Interrupt endpoint.

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6 Electrical Specifications

6.1 DC Characteristics

6.1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VCCK	Digital core power supply	-0.3 to 1.96	V
VCCA	Analog Power for USB Transceiver. 3.3V	- 0.3 to 3.63	V
VCC3IO	Power supply of 3.3V I/O	- 0.3 to 3.63	V
VCC5A	Power supply of 5V from VBUS.	- 0.3 to 5.5	V

Note: 1.Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the optional sections of this datasheet. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

2. The input and output negative voltage ratings may be exceeded if the input and output currents under ratings are observed.

6.1.2 Recommended Operating Condition

Symbol	Parameter	Min	Typ	Max	Unit
VCCK	Digital core power supply	1.62	1.8	1.96	V
VCCA	Analog Power for USB Transceiver. 3.3V	2.97	3.3	3.63	V
VCC3IO	Power supply of 3.3V I/O	2.97	3.3	3.63	V
VCC5A	Power supply of 5V for internal regulator.	4.5	5	5.5	V
Tj	Junction operating temperature	-40	25	125	℃
Ta	Commercial ambient operating temperature	0	-	70	℃
	Industrial ambient operating temperature	-40	-	85	℃

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6.1.3 Leakage Current and Capacitance

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IN}	True 3.3 V I/O input leakage current	V_{in} = 3.3 V or 0 V	-	≤±1	-	μA
	3.3 V with 5 V tolerance I/O Input leakage current	V_{in} = 5 V or 0 V	-	<±1	-	pF
C_{IN}	Input capacitance	3.3V I/O cells	-	2.25	-	pF
		3.3V with 5V tolerant I/O cells	-	3.6	-	pF

Note: C_{IN} includes the cell layout capacitance and pad capacitance (Estimated to be 0.5 pF).

6.1.4 DC Characteristics of 3.3V I/O Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vil	Input low voltage	LVTTL	-	-	0.8	V
Vih	Input high voltage		2.0	-	-	V
Vt-	Schmitt trigger negative going threshold voltage	LVTTL	0.8	1.1	-	V
Vt+	Schmitt trigger positive going threshold voltage		-	1.6	2.0	V
Vol	Output low voltage	|Iol| = 4~8mA	-	-	0.4	V
Voh	Output high voltage	|Ioh| = 4~8mA	2.4	-	-	V
Vopu[1]	Output pull-up voltage for 5 V tolerance I/O cells	PU = VCC3IO, PD = 0V, $\|I_{pu}\|$ = 1 μA	VCC3IO - 0.9	-	-	V
Rpu	Input pull-up resistance	PU = VCC3IO, PD = 0V		75		KΩ
Rpd	Input pull-down resistance	PU = 0V, PD = VCC3IO		75		KΩ

[1] This parameter indicates that the pull-up resistor for the 5 V tolerance I/O cells cannot reach the VCC3IO DC level even without the DC loading current.

6.1.5 DC Characteristics of 1.8V I/O Pin

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vil	Input low voltage	LVTTL	-	-	0.52	V
Vih	Input high voltage		1.10	-	-	V
Vt-	Schmitt trigger negative going threshold voltage	LVTTL	0.52	0.60	0.68	V
Vt+	Schmitt trigger positive going threshold voltage		0.90	1.00	1.10	V

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6.1.6 DC Characteristics of Voltage Regulator(3.3V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
REG06_VCC33	Output voltage of regulator		3.14	3.3	3.46	V
I_{load}	Driving current of regulator		-	-	80	mA
I_Q	Quiescent current consumption	I_{load} = 0mA	-	100	200	uA
$\frac{\Delta VCC33A}{\Delta VCC5AX\ VCC33A}$	Linear regulation			0.02	0.04	%/mA
$\frac{\Delta VCC33A}{\Delta I\ VCC33A}$	Load regulation		-	0.02	0.05	%/mA
Tj	Operating junction temperature		-40	25	125	ºC

6.1.7 DC Characteristics of Voltage Regulator(1.8V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
REG02_V18	Output voltage of regulator		1.71	1.8	1.89	V
I_{load}	Driving current of regulator		-	-	40	mA
I_Q	Quiescent current consumption	I_{load} = 0mA	-	100	200	uA
$\frac{\Delta VCC18A}{\Delta VCC5AX\ VCC18A}$	Linear regulation			0.02	0.04	%/mA
$\frac{\Delta VCC18A}{\Delta I\ VCC18A}$	Load regulation		-	0.02	0.05	%/mA
Tj	Operating junction temperature		-40	25	125	ºC

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6.2 Power Consumption

Symbol	Description	Conditions	Min	Typ	Max	Unit
IVCC18	Current Consumption of 1.8V	Operating at USB High speed with 4x6M serial ports		25.86		mA
IVCC33	Current Consumption of 3.3V			17.86		mA
IVCC18	Current Consumption of 1.8V	Operating at USB High speed with 4x921600 serial ports		13.47		mA
IVCC33	Current Consumption of 3.3V			16.83		mA
IVCC18	Current Consumption of 1.8V	Operating at USB High speed with 4x115200 serial ports		11.38		mA
IVCC33	Current Consumption of 3.3V			16.58		mA
IVCC18	Current Consumption of 1.8V	Operating at USB High speed susupended in remote wake up mode		0.198		mA
IVCC33	Current Consumption of 3.3V			0.165		mA
IVCC18	Current Consumption of 1.8V	Operating at USB High speed susupended without remote wake up		0.198		mA
IVCC33	Current Consumption of 3.3V			1.165		mA
IVCC18	Current Consumption of 1.8V	Operating at USB Full speed with 4x6M serial ports		20.55		mA
IVCC33	Current Consumption of 3.3V			13.02		mA
IVCC18	Current Consumption of 1.8V	Operating at USB Full speed with 4x921600 serial ports		8.10		mA
IVCC33	Current Consumption of 3.3V			12.33		mA
IVCC18	Current Consumption of 1.8V	Operating at USB Full speed with 4x115200 serial ports		6.18		mA
IVCC33	Current Consumption of 3.3V			11.25		mA
IVCC18	Current Consumption of 1.8V	Operating at USB Full speed susupended in remote wake up mode		0.198		mA
IVCC33	Current Consumption of 3.3V			0.199		mA
IVCC18	Current Consumption of 1.8V	Operating at USB Full speed susupended without remote wake up		1.198		mA
IVCC33	Current Consumption of 3.3V			0.199		mA
I_{DEVICE}	Power consumption of AX78140 full loading (chip only)	1.8V		25.86		mA
		3.3V		17.86		mA
I_{SYSTEM}	Power consumption of AX78140 full loading (demo board)	VBUS of 5.0V (With 4 transceivers operate in 921600)		99.50		mA
I_{SYSTEM}	Power consumption of AX78140 full loading (demo board)	VBUS of 5.0V (Without transceiver operate in 6M)		44.08		mA

Table 6: Power consumption

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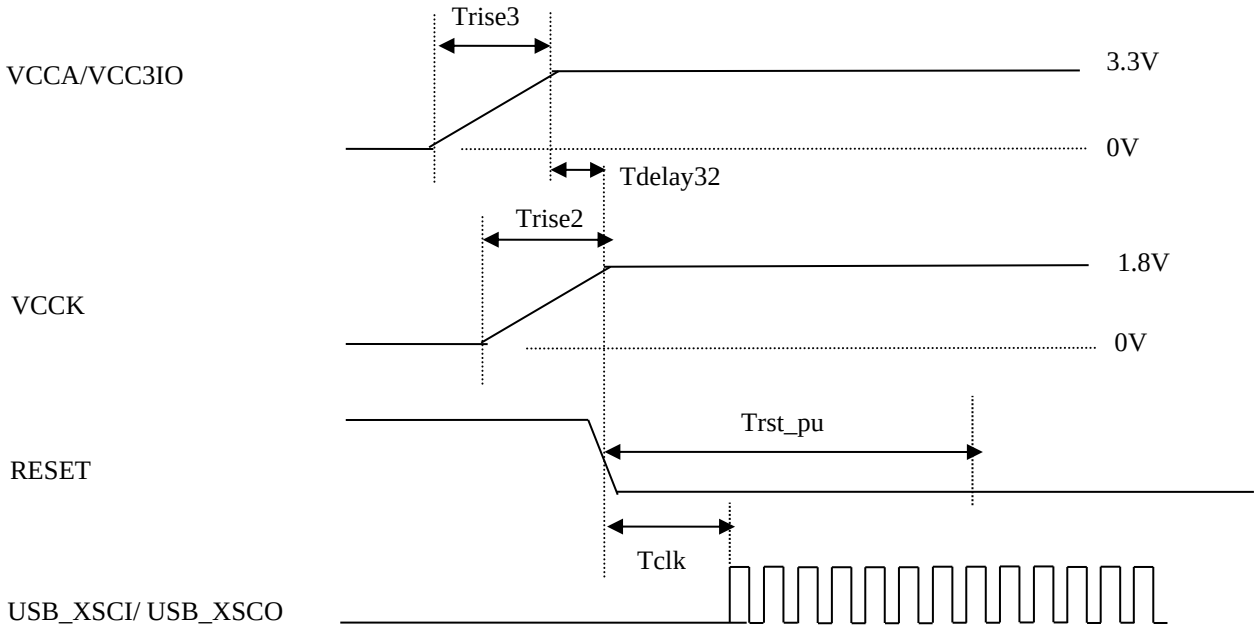
6.3 Power-up Sequence

At power-up, the AX78140 requires the VCCA/VCC3IO power supply to rise to nominal operating voltage within Trise3 and the VCCK power supply to rise to nominal operating voltage within Trise2.



Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{rise3}	3.3V power supply rise time	From 0V to 3.3V	1	-	10	ms
T_{rise2}	1.8V power supply rise time	From 0V to 1.8V	-	-	10	ms
$T_{delay32}$	3.3V rise to 1.2V rise time delay		-5	-	5	ms
T_{clk}	12MHz crystal oscillator start-up time	From VCCK = 1.8V to first clock transition of USB_XSCI	-	1	-	ms
T_{rst_pu}	RESET high level interval time from power-up	From VCCK = 1.2V and VCC3IO = 3.3V to RESET going low	T_{clk} + Trst *1	-	-	ms

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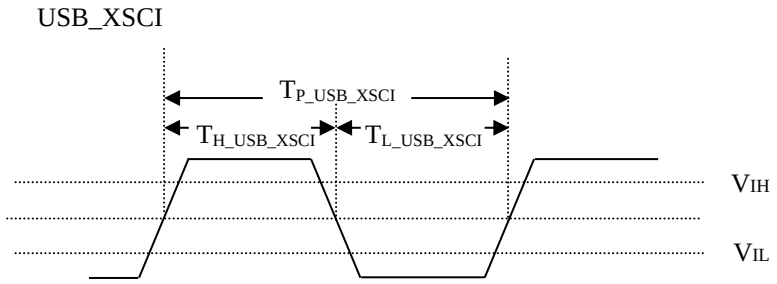
6.4 AC Timing Characteristics

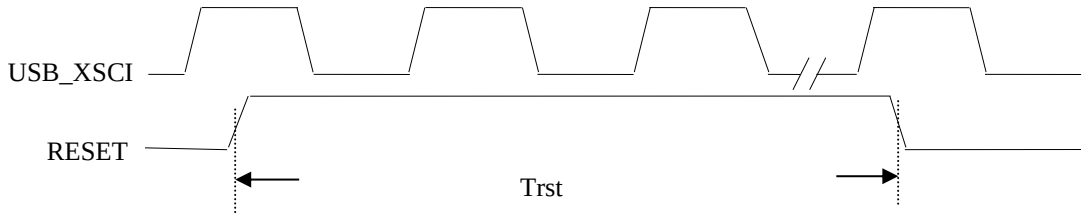
Notice that the following AC timing specifications for output pins are based on CL (Output load) equal to 50pF.

6.4.1 Clock Timing



Symbol	Parameter	Condition	Min	Typ	Max	Unit
$T_{P_USB_XSCI}$	USB_XSCI clock cycle time		-	83.33	-	ns
$T_{H_USB_XSCI}$	USB_XSCI clock high time		-	41.66	-	ns
$T_{L_USB_XSCI}$	USB_XSCI clock low time		-	41.66	-	ns

6.4.2 Reset Timing



Symbol	Description	Min	Typ	Max	Unit
Trst	Reset pulse width after USB_XSCI is running	250	-	-	USB_XSCI clock cycle

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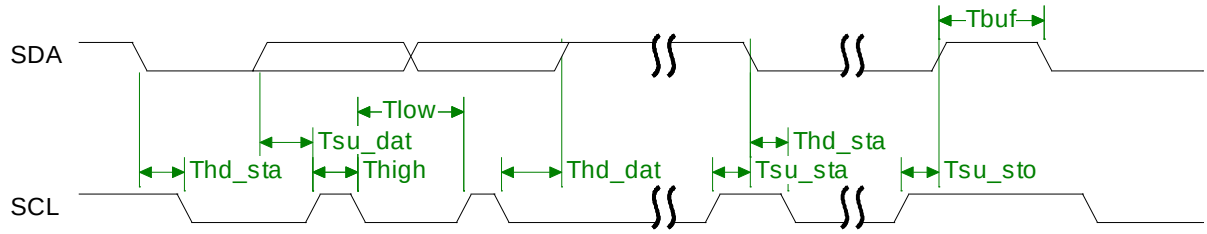
6.4.3 I²C EEPROM Timing



Symbol	Parameter	Min	Typ	Max	Units
Fclk[2]	SCL clock frequency SCL will use 100KHz during the configuration EEPROM loading and can be changed to support 400KHz operating.	-	-	100, 400	KHz
Thigh	High period of the SCL clock	-	SCL_HP+5	-	Tsys_clk[1]
Tlow	Low period of the SCL clock	-	SCL_LP+2	-	Tsys_clk
Thd_sta	Hold time of (repeated) START condition. After this period, the first clock pulse is generated	-	SHSC+1	-	Tsys_clk
Tsu_sta	Setup time for a repeated START condition	-	SHSC+1	-	Tsys_clk
Tsu_dat	Data Setup time	-	(SCL_LP/2)+1	-	Tsys_clk
Thd_dat	Data hold time	-	(SCL_LP/2)+1	-	Tsys_clk
Tsu_sto	Setup time for STOP condition	-	SCL_HP+5	-	Tsys_clk
Tbuf	Bus free time between a STOP and START condition	-	(SCL_HP/2)+BFT+2	-	Tsys_clk

Note 2: Fclk = 1/Tclk, where Tclk = ((SCL_HP + SCL_LP) * Tsys_clk). The SCL_HP and SCL_LP are I²C SCL Period Register.

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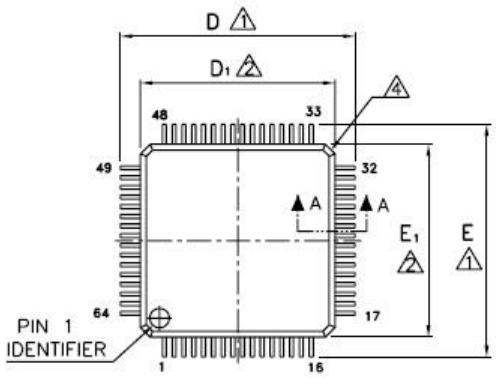
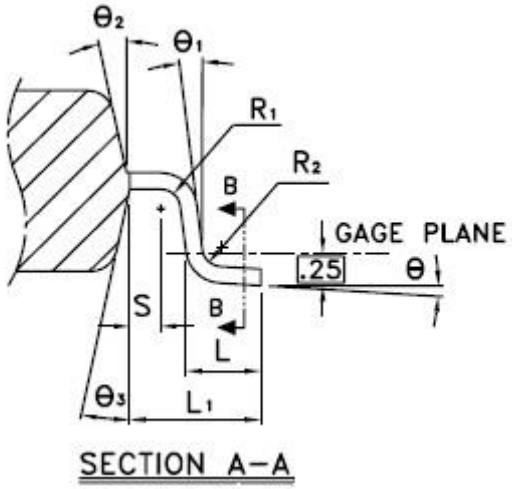
7 Package Information

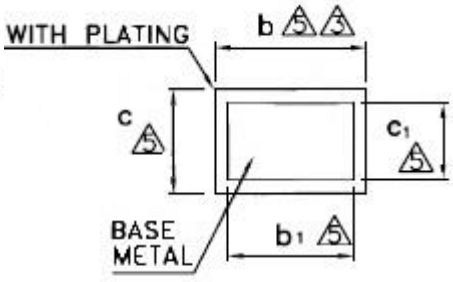
7.1 64-pin LQFP 10x10 package

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.012	0.015	0.018
b_1	0.17	0.20	0.23	0.012	0.014	0.016
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	12.00 BSC			0.472 BSC		
D_1	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E_1	10.00 BSC			0.394 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	12°TYP			12°TYP		
$θ_3$	12°TYP			12°TYP		





SECTION A–A



SECTION B–B

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8 Ordering Information

Part Number	Description
AX78140 LI	64-pin LQFP lead Free package, industrial temperature range: -40 to 85°C.

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9 Revision History

Revision	Date	Comment
V0.10	2016/05/19	Prelimiary release.
V0.20	2016/06/03	1. Modified some descriptions in Section 6.1.2, 6.2.
V0.21	2016/10/11	1. Corrected typos in Section 8.
V1.00	2017/04/26	1. Corrected a typo on the RESET_SEL pin I/O Type in Section 2.1.
V1.01	2017/08/18	1. Added Section 6.1.5 “DC Characteristics of 1.8V I/O Pin”. 2. Corrected a typo in Section 2.1.
V1.10	2017/12/07	1. Modified Features, Section 2.1 to add the software controlled GPIO descriptions. 2. Added Section 3.12 “GPIO”.
V1.11	2018/08/03	1. Added Section 6.1.6 & 6.1.7
V1.20	2024/01/17	1. Removed AX78140 LF information in Section 1 and 8.

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