AX58100 EtherCAT Slave Controller Application Design Note

Revision 1.05
August 6th, 2021

Revision History

Revision	Date	Description
0.10	2018/05/18	Preliminary release
1.00	2018/11/23	1. Added Section 4 “Ethernet PHY Selection Considerations”.
1.01	2018/12/04	1. Corrected some typos in Section 3. 2. Modified some descriptions in Section 4 and 8. 3. Updated Figure 3.
1.02	2020/05/26	1. Modified some descriptions in Section 2 & 11
1.03	2020/11/13	1. Updated Figure 5, Figure 6, Figure 12 & Figure 13.
1.04	2021/01/22	1. Updated Figure 2 & 5 & 11 & 12.
1.05	2021/08/06	1. Updated some description in Section 3.

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1. Introduction

The AX58100 is a 2/3-port EtherCAT Slave Controller (ESC), licensed from Beckhoff Automation, with two integrated Fast Ethernet PHYs which support 100Mbps full-duplex operation and HP Auto-MDIX. The AX58100 provides a cost-effective solution for industrial automation, motion/motor/digital I/O control, Digital to Analog (DAC)/Analog to Digital (ADC) converters control, sensors data acquisition, robotics, etc. industrial fieldbus applications.

This document indicates important information about external components selection, schematic and PCB layout design notes. ASIX Electronics highly recommends designers to read through this design note firstly before starting the hardware designs.

2. EEPROM Selection & Bootstrap Pins Considerations

The AX58100 supports I²C EEPROM with EEPROM size from 1 Kbit (128 bytes) to 4 Mbit (500Kbytes). The AX58100 HWCFGEE contents from offset 0x00 to 0x7F are mandatory, as well as the general category (at least minimum I²C EEPROM size is 2Kbit, and for the complex devices with many categories should be equipped with 32 Kbit EEPROMs or larger). Please refer to Section 3 of AX58100 datasheet to select a proper I²C EEPROM part based on AX58100 pin #19 LED_RUN/EEP_SIZE bootstrap configuration.

Pins	Signal Name	Description
19	EEP_SIZE	I²C EEPROM Size 0: 1 Kbit to 16Kbit 1: 32Kbit to 4Mbit

The following is the I²C EEPROM reference circuit of AX58100 applications.

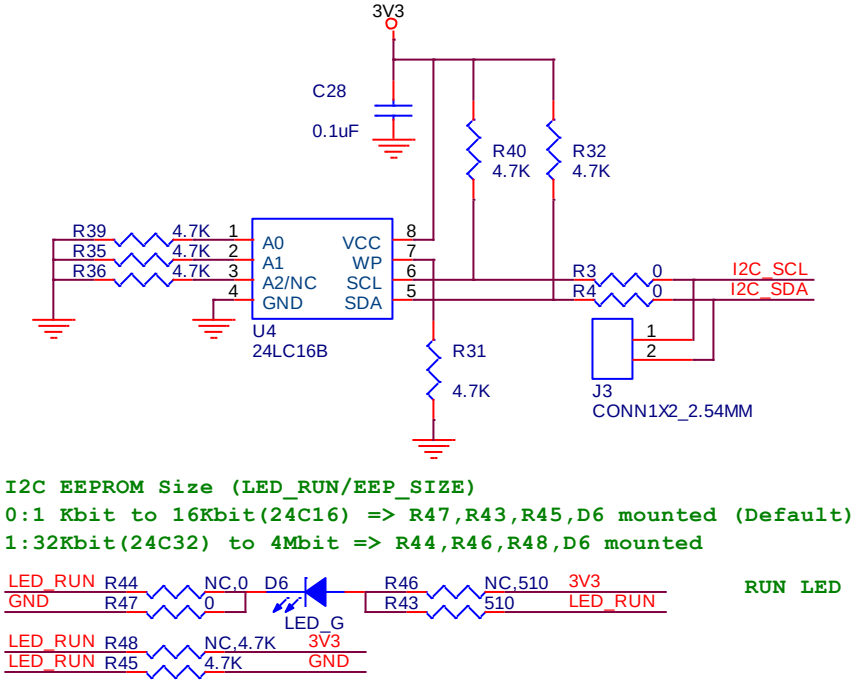


Figure 1. I²C EEPROM Reference Circuit

The AX58100 supports five multi-function bootstrap pins (pin 19, 20, 58, 40, and 41) for five hardware configurations, i.e. external I²C EEPROM size, ESC supported port number, RSTO polarity and integrated port 0/1 PHY media mode; and it also supports other three multi-function bootstrap pins (pin 42, 52, 66) for the configuration of port 2 MII signals. User needs to utilize an external resistor to pull up / down these bootstrap pins.

Pins	Signal Name	Description
19	EEP_SIZE	I²C EEPROM Size 0: 1 Kbit to 16Kbit 1: 32Kbit to 4Mbit
20	3PORT_MODE	ESC port number 0: 2 ports mode 1: 3 ports mode
58	RSTO_POL	RSTO Reset Output Polarity 0: Active Low 1: Active High
61	PDI_EMU	Device emulation (0x0141.0) 0: Device status register is controlled by PDI 1: Device status register is identical to device control register
40	P0_FIBER	Port 0 PHY media mode 0: Copper mode 1: Fiber mode
41	P1_FIBER	Port 1 PHY Media mode 0: Copper mode 1: Fiber mode
66	TX_SH [1]	Port 2 MII TXD Align position 2'b00: Align with MCLK, 2'b01: Delay 1/4 phase with MCLK 2'b10: Delay 1/2 phase with MCLK 2'b11: Delay 3/4 phase with MCLK
42	TX_SH [0]	
52	LINK_POL	Port 2 MII LINK Polarity 0: Active Low 1: Active High

Figure 2. AX58100 Bootstrap Pins Reference Circuit

Note: The SD signal should be connected to GND through a 4.7K resistor in Copper mode.

3. Crystal Selection Considerations

The following are the specification of NSK NXK25.000AE12F-KAB6-12 SMD 25MHz crystal with CL 12pF, ESR 40 Ohm and Drive Level 100uW.

Parameter	Symbol	Typical Value
Nominal Frequency	Fo	25.000000MHz
Oscillation Mode		Fundamental
Frequency Tolerance (@25℃)		±20ppm
Equivalent Series Resistance	ESR	40 Ohm max.
Load Capacitance	CL	12pF
Drive Level		100uW
Operation Temperature Range		-40℃ ~ +105℃
Aging		±3ppm/year

The following is an example of the 25MHz crystal clock circuit. The 1M feedback resistor is optional for 25MHz crystal circuit. Please reserve the R22, R23 resistors circuit for flexible designs.

25MHz +/- 30ppm Crystal

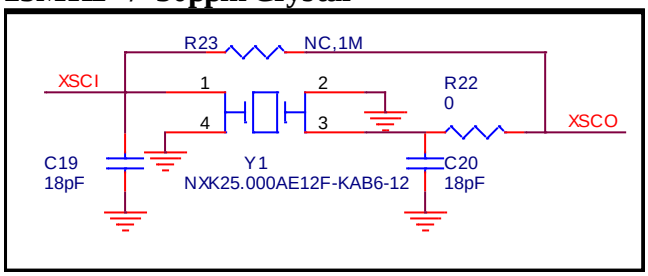


Figure 3. 25MHz Crystal Reference Circuit

Note:

1. Please make sure the XSCO 25MHz clock output signals are within 25MHz +- 25ppm. If the XSCO 25Mhz clock output signals are out of the specification, please fine-tune the load capacitors (C19, C20) to meet the specification.
2. If you want to use the oscillator as 25MHz clock source, please select a 1.2 voltage level oscillator in your application.

4. Ethernet PHY Selection Considerations

The AX58100 ESC which is licensed from Beckhoff Automation supports two embedded PHYs and an optional MII interface for flexible network topology. The optional MII interface of AX58100 ESC is optimized for low processing/forwarding delays by omitting a transmit FIFO. To allow this, the ESC has additional requirements to Ethernet PHY, which is easily accomplished by several PHY vendors. Please refer to ***Beckhoff's PHY Selection Guide*** to select a proper Ethernet PHY.

The following is the principle connection between AX58100 ESC optional MII interface and Ethernet PHY. The clock source of the Ethernet PHYs and ESC must be the same quartz. The TX_CLK is not connected because the ESCs do not incorporate a TX FIFO. The TX signals can be delayed inside the ESC by setting AX58100 TX_SH[1:0] bootstrap pins for TX_CLK phase shift compensation. The LINK is connected to the PHY LED output indicating a 100 Mbps (Full Duplex) link.

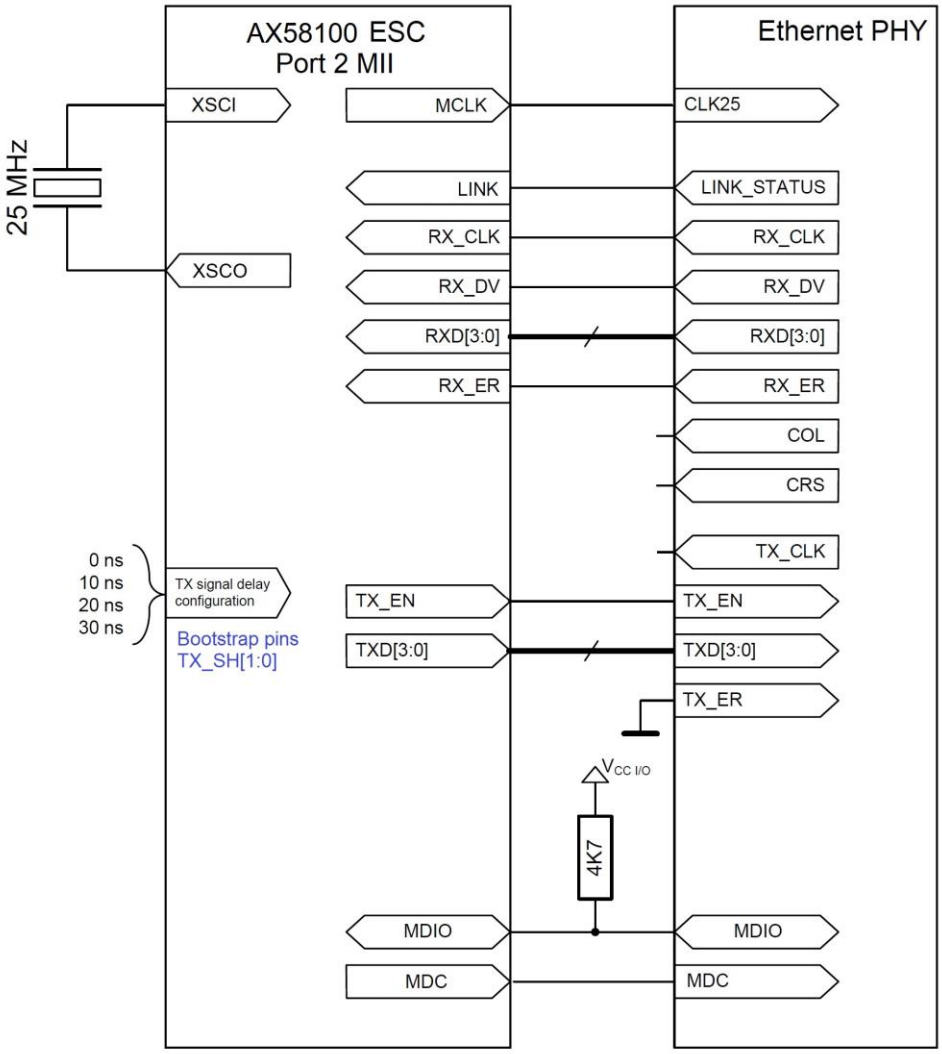


Figure 4. The principle connection between AX58100 ESC optional MII interface and Ethernet PHY

5. Ethernet Magnetic Selection Considerations

5-1. RJ-45 + Transformer without Auto-MDIX

The following is an example reference circuit of RJ-45 + Transformer (Turns Ratio 1CT:1CT) without Auto-MDIX function. The TCT and RCT pins of the Ethernet magnetic without Auto-MDIX function are separate inside; these two pins CANNOT be shorted together.

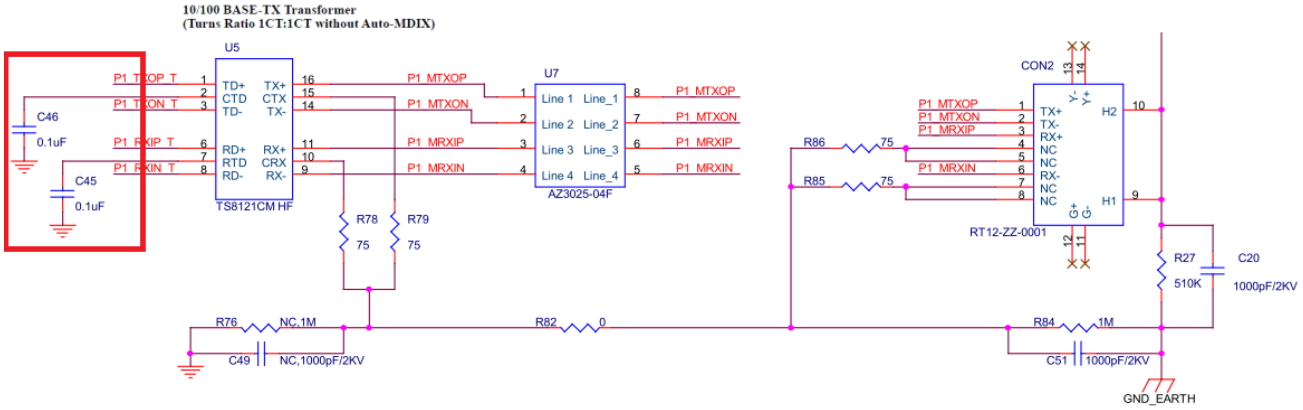
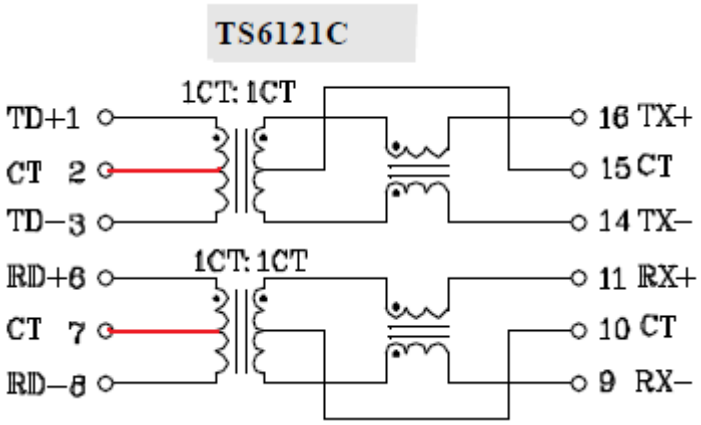


Figure 5. RJ-45 + Transformer Reference Circuit

The following is an example (Bothhand TS6121C) of 10/100 Base-TX Ethernet transformer without Auto-MDIX function.



6. 4-Layer PCB Design

We strongly suggest customers to design AX58100 on the printed circuit board (PCB) with at least 4 layers. The 4-layer PCB design can help reduce some potential EMI, thermal and signal integrity issues, etc.

The following is an example of 4-Layer PCB design.

Layer 1	Component (Top)	Magnetic and major signals
Layer 2	Ground	Digital/analog ground planes
Layer 3	Power	Digital/analog power planes
Layer 4	Component (Bottom)	Magnetic and other signals

Figure 6. An Example of 4-Layer PCB Design

7. Power and Ground Planes Considerations

1. Digital GND and Analog GND can be placed together in one-piece so as to enlarge the GND, and thus helping dissipation of noises.
2. The RJ-45 chassis ground and the digital ground should be isolated through a 1206 1M ohm resistor and a 1206 0.1uF/2KV decoupling capacitor, and the gap between the 1206 package should be larger than 60 mils.

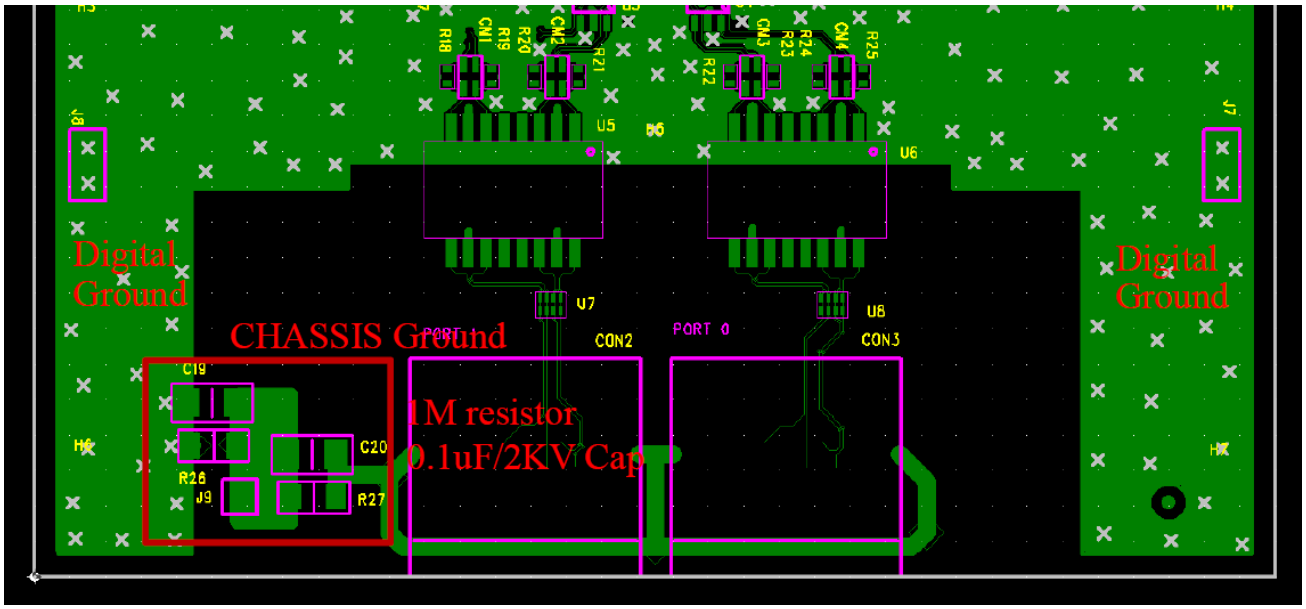


Figure 7. Typical Chassis/Digital Ground Planes

3. All the digital and analog power planes for different voltage supplies should be handled separately with different blocks to supply power to IC chip and peripheral components.

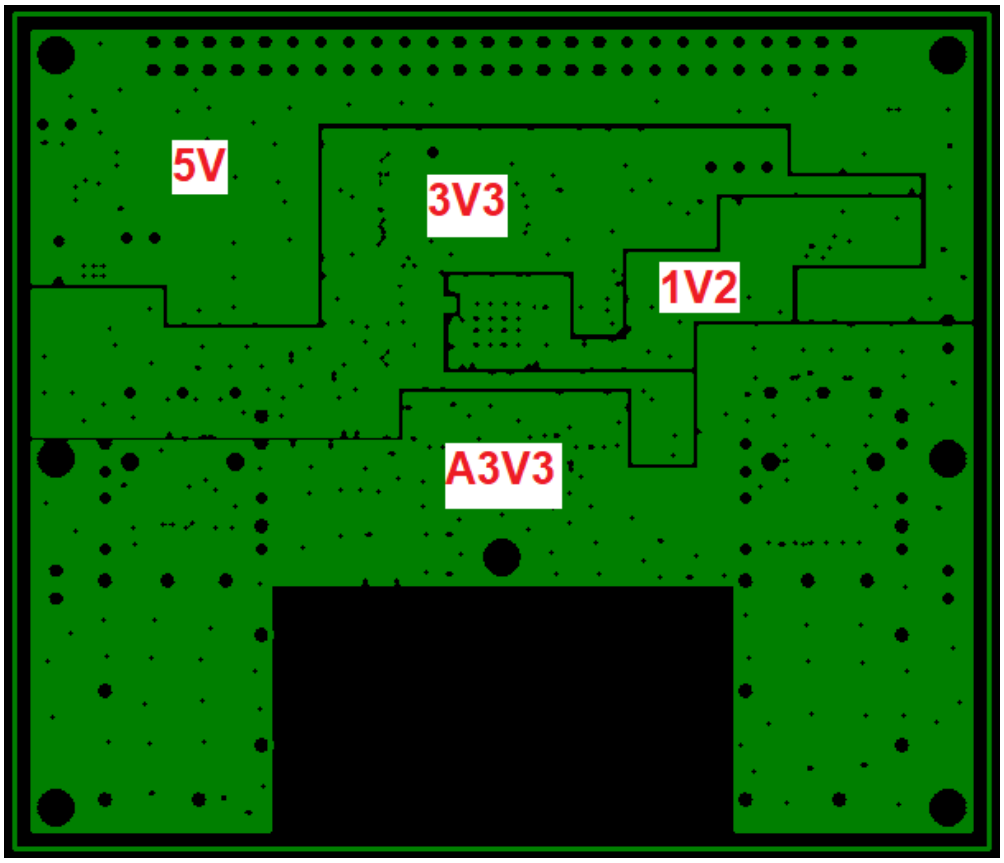
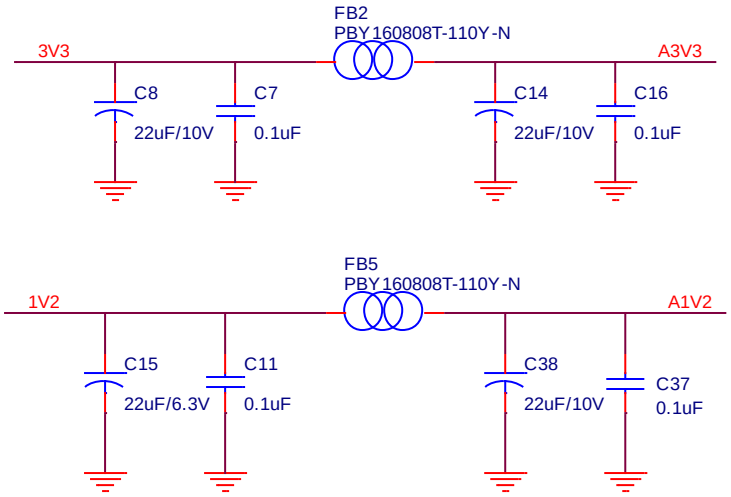


Figure 8. Typical Digital/Analog Power Planes for Single RJ-45 with Integrated Magnetic

Note: The above figures are the Digital and Analog Power Planes diagram of an illustrative PCB board design. For exact layout pattern, ASIX Electronics provides the PCB layout and Gerber files of AX58100 EVB for customer reference.

4. The digital and analog power planes should be isolated with a Ferrite Bead to isolate the noise source, and all power planes should be implemented with a large compensating capacitor to provide a stable power source.



5. All power pins should be implemented with a decoupling capacitor, and the decoupling capacitor should be as close to the respective power pin of AX58100 as possible.

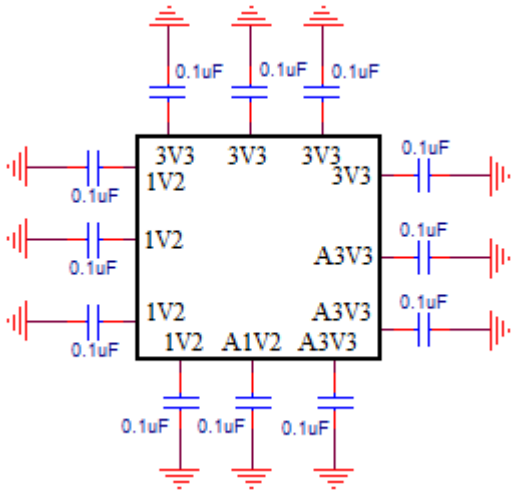


Figure 9. An Example of Power Pins and Decoupling Capacitors Circuits

8. Ethernet Magnetic Layout Considerations

This section describes some general Ethernet layout considerations for the differential signals of the Ethernet controller, the Ethernet magnetic and the RJ-45 connector.

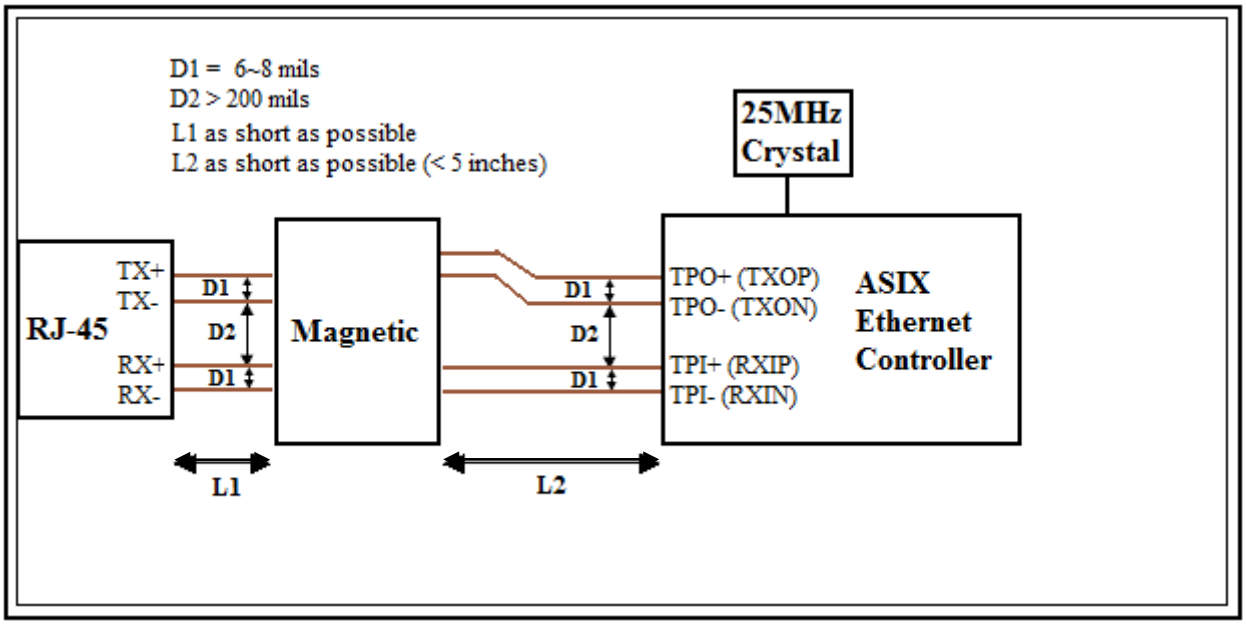
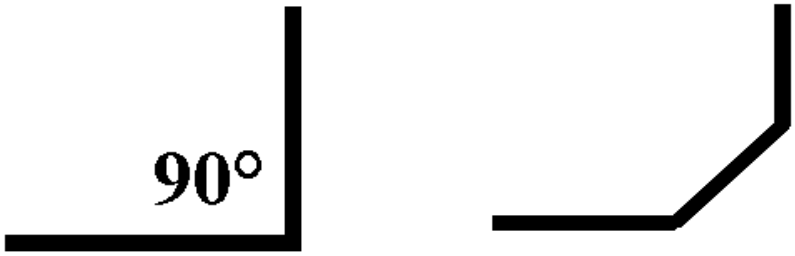


Figure 10. Ethernet TX± and RX± Differential Pairs Layout

1. The ideal Ethernet differential impedance between TX + and TX- traces (between RX+ and RX-) should be 100 Ohm. The Ethernet differential impedance between the TX+/TX-/RX+/RX- trace and GND should be 50 Ohm respectively. The designer can use the trace width of TX+/TX-/RX+/RX- traces to fine tune the Ethernet differential impedance value (a wider trace has a smaller impedance value). If the PCB manufacturer provides TDR measurement, it helps control the PCB Impedance.
2. The crystal clock source and the switching noises from digital signals should be kept away from the TX± and RX± differential pairs.
3. The Ethernet magnetic should be placed as close to the RJ-45 connector as possible.
4. The Ethernet controller should be placed as close as possible to the magnetic. If there are some limitations on the PCB layout, the trace length from the Ethernet controller to the magnetic should not be longer than 5 inches.
5. The TX± and RX± differential pairs should be routed as close as possible. The trace spacing D1 between TX+ and TX- (or between RX+ and RX-) pair should be in 6 ~ 8 mils. The trace width should be adjusted accordingly to yield the required trace impedance.
6. The spacing D2 between the TX± and RX± differential pairs should be larger than 200 mils. If the PCB layout is really difficult to meet this requirement, the D2 spacing should be as larger as possible.
7. Route the TX± and RX± differential pairs as straight as possible and keep them in parallel for differential pairs.
8. Keep the trace length difference between the TX+ and TX- (or RX+ and RX-) pair within 700 mils.

9. Route the TX± and RX± differential pairs running symmetric, equal length and close whenever possible.
10. Avoid using vias on the traces of the TX± and RX± differential pairs. If the PCB layout really needs to use vias on the differential pairs, please match the vias to keep the differential pairs balanced.
11. The power plane and digital ground plane should not be placed under the magnetic and RJ-45 connector.
12. Avoid routing the signal trace with right angle, instead, the signal trace should be routed with multiple 135° angles.



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9. Thermal Considerations

This section describes some information about how to reduce the operating temperature on the AX58100 applications.

9-1. Improve the Cooling Plane

There are two major heat sources on the AX58100 applications. One is the AX58100 controller and the other is the external voltage regulator.

You can connect the VCC/GND pins of the AX58100 controller with wide traces to the respective power/ground planes to increase the cooling effect and reduce the operating temperature of the AX58100 controller.

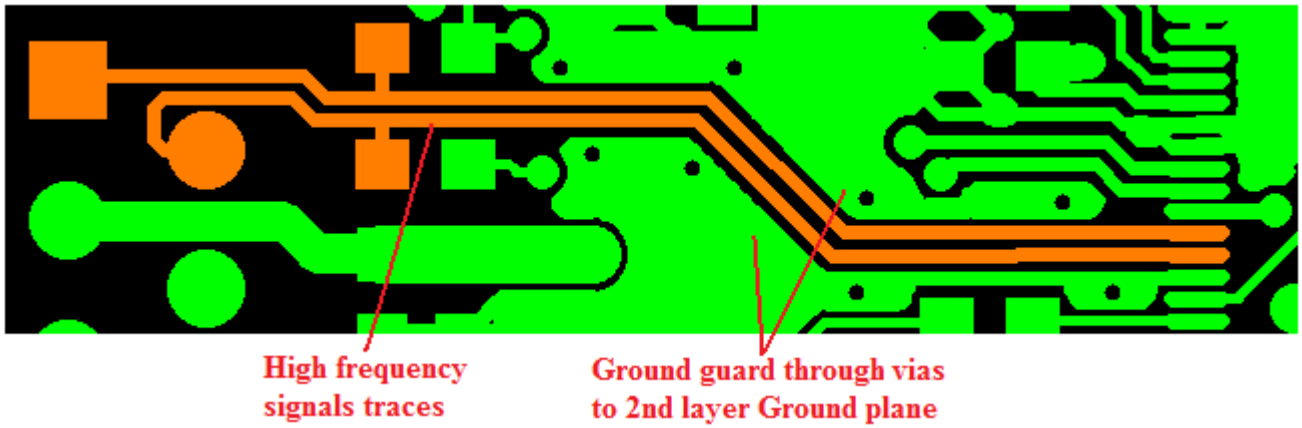
You can also add a cooling plane for the external voltage regulator to reduce the operating temperature of the external voltage regulator.

9-2. Improve the Air Convection

You can place the AX58100 controller at the location with good air convection and stay away from the high-operating-temperature IC such as voltage regulator or external MCU/DSP to reduce the operating temperature of the AX58100 controller.

10. EMI Considerations

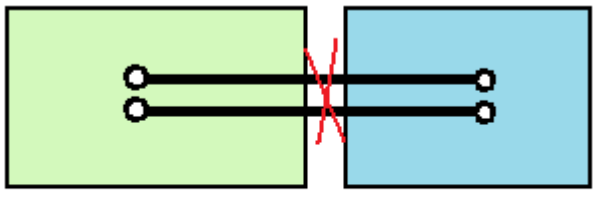
1. The high frequency signals traces such as Ethernet differential signals, clock signals, etc. shall be surrounded by GND to prevent interference to other signal wires. Better EMI effect can be attained by a one-piece GND underneath the IC furnished with PTH holes to enlarge the GND area.



2. The chosen connector must be shielded so that EMI integrity of the design is not compromised. The shield must be electrically connected to chassis ground to extend the chassis barrier for high frequency emissions. If an unshielded connector were used, the EMI would pass through the nylon material of the connector. The shield will also prevent less external EMI from entering the chassis.

3. To reduce electromagnetic emissions and susceptibility, it is imperative that traces from the transceiver to the magnetic sand from the magnetic to the RJ-45 be routed as differential pairs. The objective is to close the loop area formed by the two conductors. The radiated field from the loop or the voltage picked up by the loop by external fields is governed by the field strength and the area formed by the two conductors. Reasonable board design uses 5~10 mils trace widths separated by 10 mils. Transmit differential pairs should be routed adjacent to a VDDO power plane.

4. To avoid crossing any signal traces over any reference plane cuts; otherwise, it might cause some unpredictable EMI problems.



5. It is essential to maintain the continuous stable ground plane when board design to protect EMI emissions. The PCB designer should look upon the path currents, which take on the ground reference plane, and reduce the loop area. The continuous ground plane helps provide for a low inductance signal return path, and helps maintain a stable power supply. Simply, the most effective method of reducing EMI causes is to decrease the loop area. The main target of ground plane is designed to carry DC current only. Do not use this area as a return path for high speed signals.

11. ESD, EFT and Surge Considerations

This section describes some information about the ESD, EFT and Surge design guideline. Users can refer to the following circuit to avoid the ESD, EFT and Surge issue.

The high-energy pulses can cause abnormal system behavior and/or damage the silicon chips. The high energy can enter the system through the RJ-45 cable. There are eight wires in the RJ-45 cable and are grouped into 4 pairs as 2 active pairs (pin 1,2 & 3,6) and 2 unused pairs (pin 4,5 & 7,8).

If the high energy enters the system through the active pairs (pin 1,2 & 3,6) of RJ-45 cable, the Ethernet transformer will isolate the high energy. The unwanted high energy will be redirected to Chassis ground through a high voltage capacitor (2KV). If the high energy enters the system through the unused pairs (pin 4,5 & 7,8) of RJ-45 cable, these pins are connected to Chassis ground through a high voltage capacitor (2KV) so the unwanted high energy will be redirected to Chassis ground too.

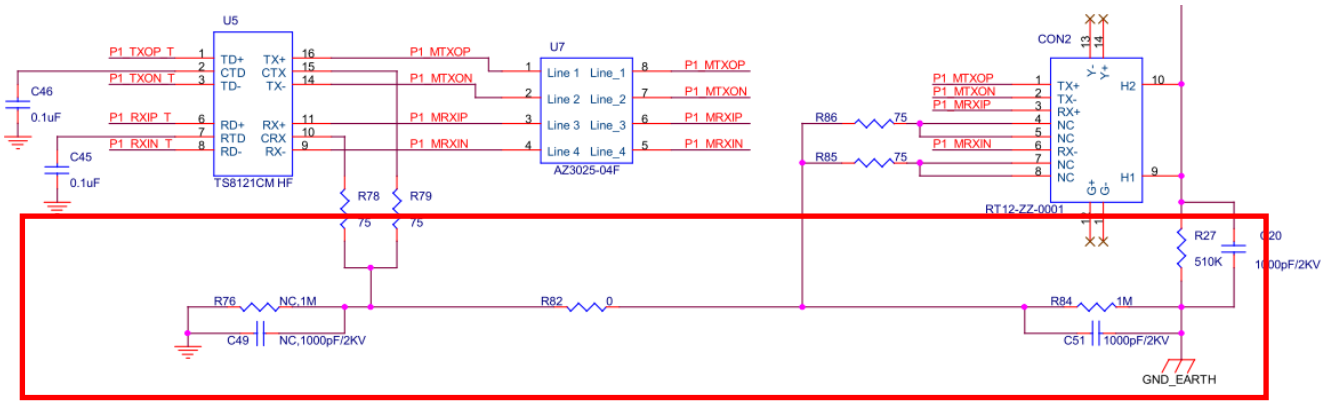


Figure 11. An Example of Separated Magnetic and RJ-45 Connector Magnetic Circuit for ESD, EFT Considerations

The fatal discharge may generate from a charged Ethernet cable, or out from outside devices such as human body, etc. Ethernet ICs become vulnerable to damage from Electrostatic Discharge within those unpredictable factors. Protecting Ethernet interfaces from cable discharges can create a challenge for board designers. Be sure a good protective circuit must effectively fasten a transient to a safe voltage, and must present an acceptable capacitive load on high-speed differential transmission lines as well.

Below are some sample circuits for ESD, EFT protection. Please refer to the ESD, EFT Protection TVS Diode datasheet for detailed ESD, EFT protection circuit.

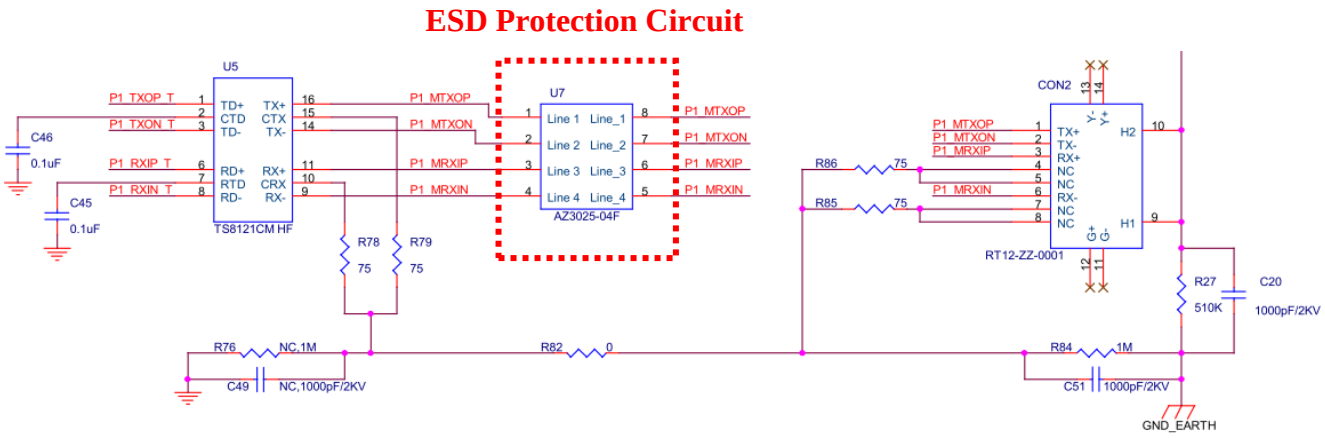


Figure 12. A Sample ESD, EFT Protection Circuit for Separate RJ-45 + Magnetic

The EthertCAT system is usually connected to an external DC power supply to provide power to the EtherCAT modules. The input protection circuits are required to protect the EthertCAT system from various faults that may occur either on the field or the EthertCAT system side.

The isolated DC-DC converter ESD, EFT and Surge protection solution is shown in Figure 13. It requires only a single isolated DC-DC converter to protect the EtherCAT system from ESD, EFT and Surge.

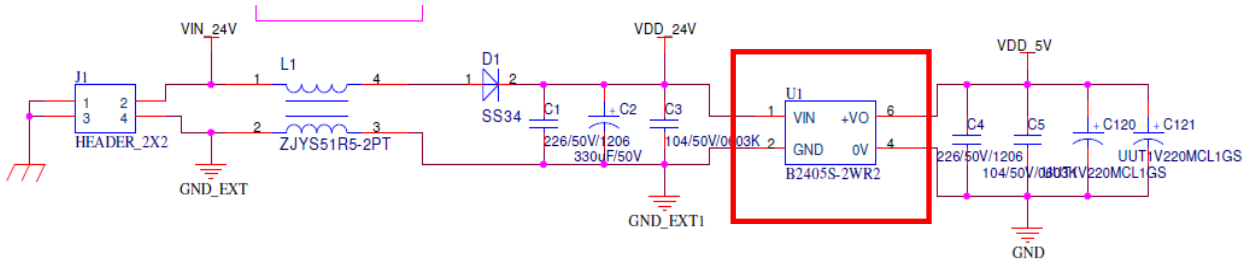
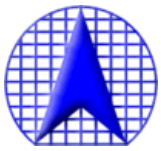


Figure 13. A Sample of isolated DC-DC converter for ESD, EFT and Surge Protection



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