MCS99xx PCB Layout Guide

Revision 1.00
Sep. 28th, 2011

Revision History

Revision	Date	Description
1.00	2011/09/28	Initial release

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1. Introduction

The MCS99xx family is a single lane PCI Express based multifunction peripheral controller which supports Multi-port UART Controller, Parallel Port Controller, Cascade Controller, GPIO Controller, an I^2C Controller and a bridge to control the transfers between the interfaces and PCIe.

This document provides guidelines for designing MCS9900, MCS9901, MCS9904 and MCS9922 PCB's. The following, component placement, and layout guidelines for PCIe Connector in designing a robust system with the MCS99xx family.

Please refer to ASIX I/O Connectivity PCIe Bridge MCS99xx products web pages (http://www.asix.com.tw/products.php?op=ProductList&PLine=74&PSeries=110) for details.

2. Functional Block Diagram

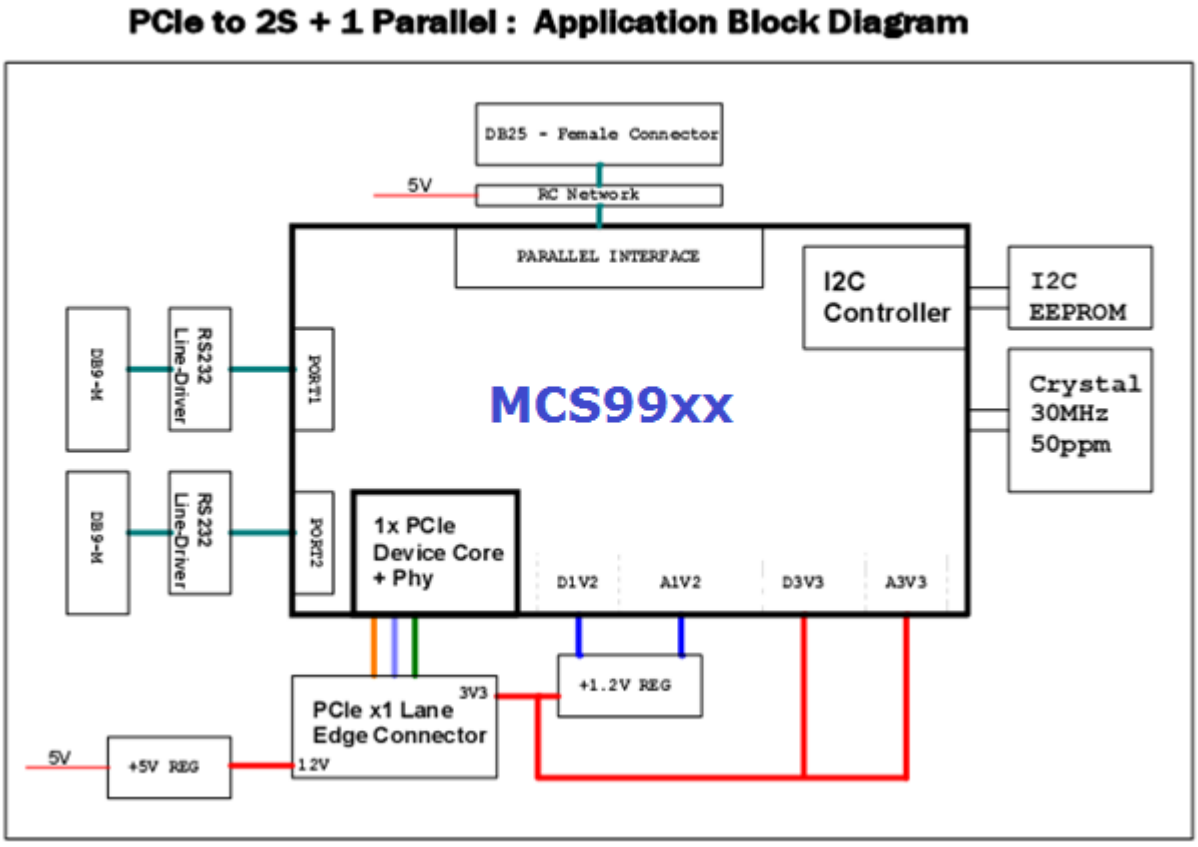

Figure 1. Example of MCS99xx 2S1P Block Diagram

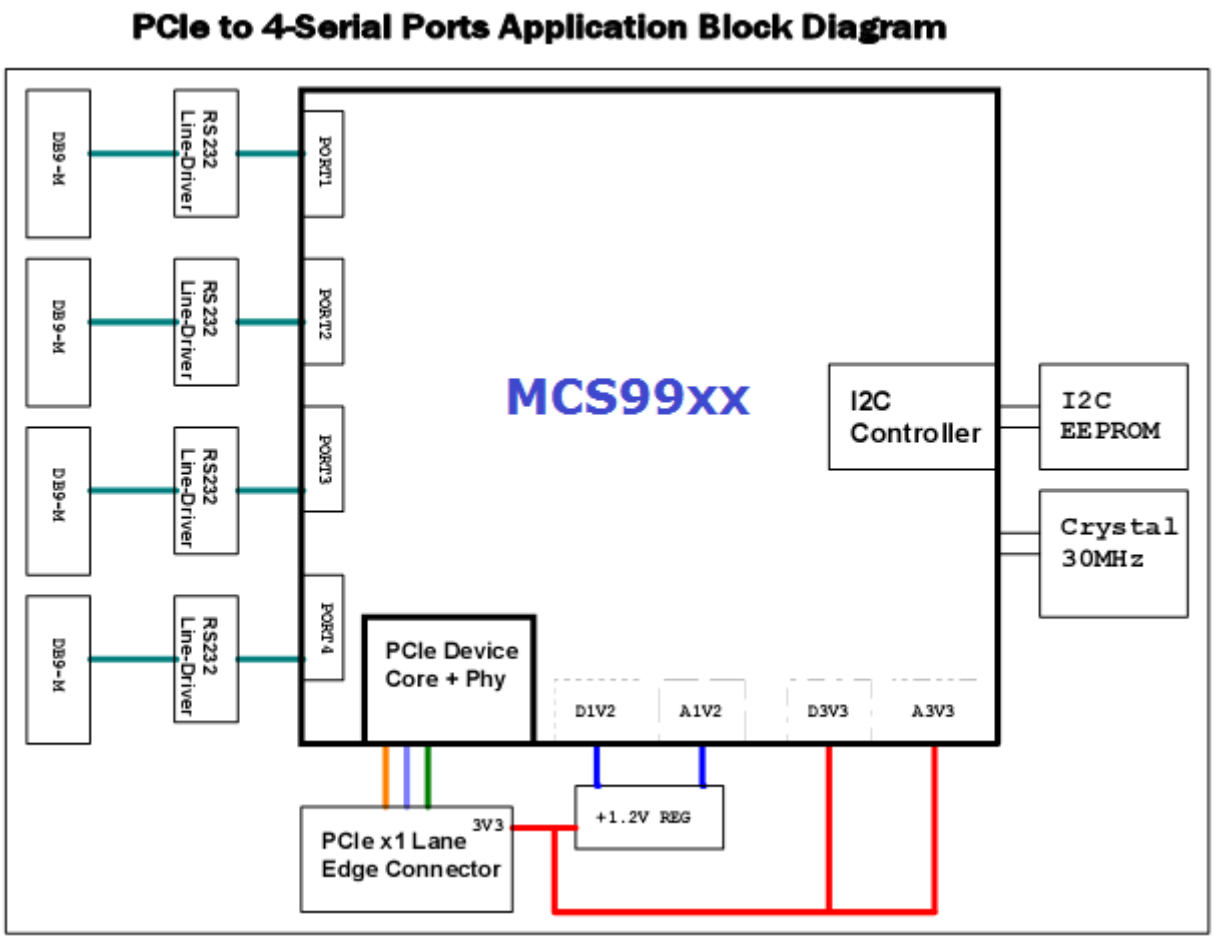

Figure 2. Example of MCS99xx 4S Block Diagram

3. Placement Suggestions

Figure 3 shows the placement suggestion, for optimum layout with minimum layer count

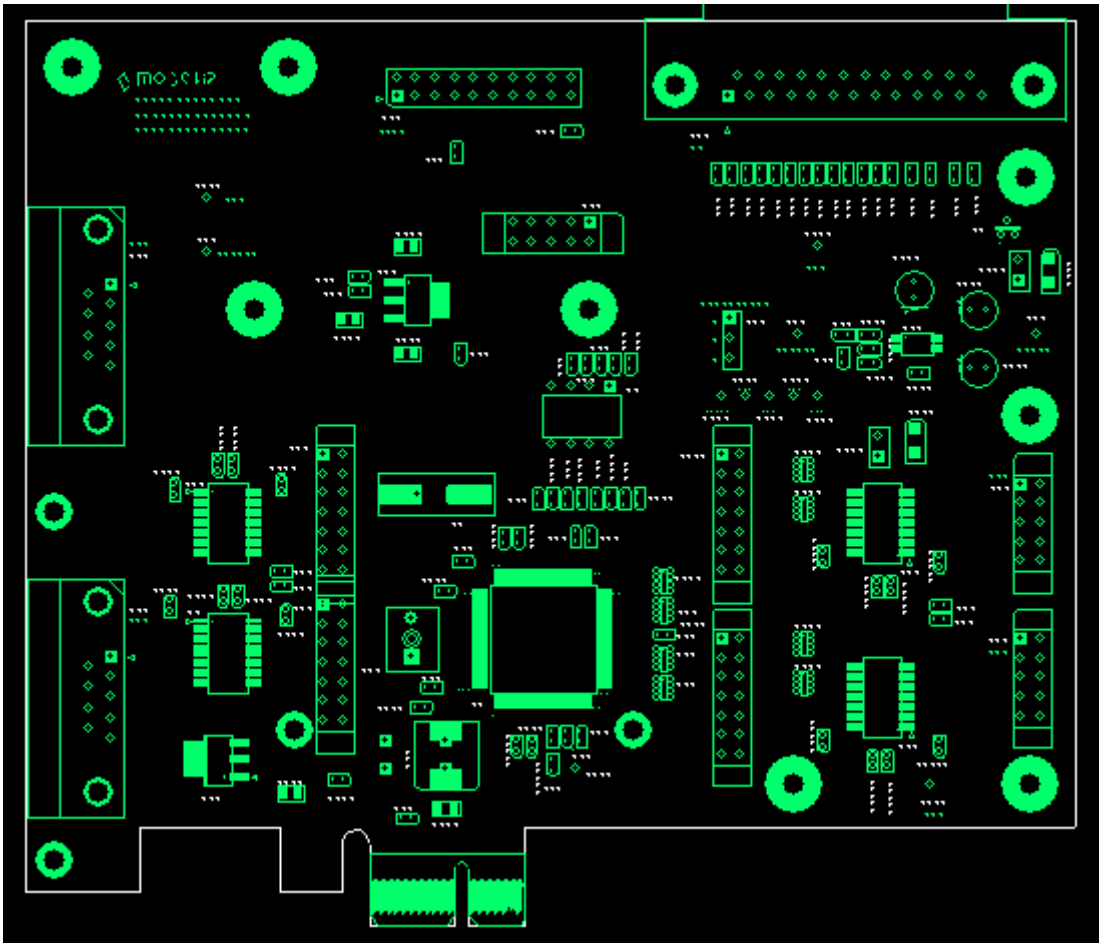

Figure 3. Placement Suggestion

4. PCB Stack-up

Table – 1 : PCB Construction / Layer Stack-up						
	Layer Name	**Type**	**Material**	**Thickness (mm)**	**Single ended Impedance**	**Differential Impedance**
		COPPER PLATING	Coating	0.0325		
L1	TOP	Conductor	Copper	0.0175	For single ended signals, 50 Ohms	a) 100 Ohms for PCIe Signals.
		Dielectric	FR4	0.10922		
L2	GND	Plane	Copper	0.035		
		Dielectric	FR4	1.1938		
L3	VCC	Plane	Copper	0.035		
		Dielectric	FR4	0.10922		
L4	BOTTOM	Conductor	Copper	0.0175	For single ended signals, 50 Ohms	a) 100 Ohms for PCIe Signals.
		COPPER PLATING	Coating	0.0325		
Total PCB Thickness in mm				**1.58224**		

Note: PCB stack-up details given above are used with MCS9900-EVB by ASIX. Data given in the above table is for reference purpose only.

5. PCIe Layout Guidelines

- Each differential signal pair must be 100 ohms differential impedance with each single-ended lane measuring in the range of 50 ohms to 55 ohms impedance to ground.
- The differential signal trace must be length matched to minimize jitter. This length matching requirement applies only to the P and N signals within a differential pair. The transmitter differential pair does not need to be length matched to the receiver differential pair.
- The differential signal pairs must not be routed over gaps in the power planes or ground planes. This causes impedance mismatches.
- Avoid routing differential pairs adjacent to noisy signals lines or high speed switching devices such as clock chips.

6. Power Supply Design

Power Supply design is perhaps the most challenging aspect of the entire process of controlling noise and radiation in high-speed design. This is largely because of the complexity of the dynamic load switching conditions. The dynamic switching characteristics very much depend upon on the actual system design and layout.

The following are some of the important issues that must be addressed during the power supply design process

- Power supply transient response, such as load regulation, line regulation, power supply ripple, power supply noise rejection.
- Power supply decoupling to ensure minimum voltage droop at the pins of the high speed design.

Excessive power supply noise can have the following harmful effects

- Voltage droop, inadequate decoupling capacitors, or current starvation may cause random logic failures. This is very difficult to debug and may even require re-design of the system to get rid of the noise.
- Inadequate voltage regulation can cause reliability problems
- Follow the layout guide-lines of power regulator manufacturer strictly for optimum layout and low power noise levels. This is key for stable high speed system design.
- Select a regulator with at least two times the maximum current capability. This provides adequate margin to handle the dynamic current condition.
- Be careful with the current starvation condition. During startup, the surge current may exceed the maximum limit of the regulator for a short period of time. The selected regulator should have a soft start capability to prevent thermal or over-current conditions from occurring.
- Add as many decoupling capacitors as space allows.

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