AX88772A/AX88172A
Low-pin-count
USB 2.0 to 10/100M Fast Ethernet Controller

Features

- Single chip USB 2.0 to 10/100M Fast Ethernet controller – AX88772A
- Single chip USB 2.0 to MII, single chip MII to Ethernet and USB Bridging controller in Dual-PHY mode (US Patent Pending) – AX88172A

- **USB Device Interface**
  - Integrates on-chip USB 2.0 transceiver and SIE compliant to USB Spec 1.1 and 2.0
  - Supports USB Full and High Speed modes with Bus-Power or Self-Power capability
  - Supports 4 or 6 programmable endpoints on USB interface
  - High performance packet transfer rate over USB bus using proprietary burst transfer mechanism (US Patent Approval)
  - Supports USB to Ethernet bridging or vice versa in hardware

- **Fast Ethernet Controller**
  - Integrates 10/100Mbps Fast Ethernet MAC/PHY
  - IEEE 802.3 10Base-T/100Base-TX compatible
  - Supports twisted pair crossover detection and auto-correction (HP Auto-MDIX)
  - Embedded 16KB SRAM for RX packet buffering and 8KB SRAM for TX packet buffering
  - Supports both Full-duplex with flow control and Half-duplex with backpressure operation
  - Supports 2 VLAN ID filtering, received VLAN Tag (4 bytes) can be stripped off or preserved
  - MAC/PHY loop-back diagnostic capability

- **Support Wake-on-LAN Function**

Product Brief

  - Supports Suspend mode and Remote Wakeup via Link-up, Magic packet, MS wakeup frame and external pin
  - Optional PHY power down during Suspend mode

- **Versatile External Media Interface**
  - Optional MII interface in MAC mode allows AX88172A to work with external 100Base-FX Ethernet PHY or HomePNA PHY
  - Optional Reverse-MII or Reverse-RMII interface in PHY mode allows AX88172A to work with external HomePlug PHY or glueless MAC-to-MAC connections
  - Optional Reverse-MII interface in Dual-PHY mode (US Patent Pending) allows AX88172A to act as an Ethernet PHY or USB 2.0 PHY for external MAC device that needs Ethernet and USB in system application

- Supports 256/512 bytes (93c56/93c66) of serial EEPROM (for storing USB Descriptors)
- Supports automatic loading of Ethernet ID, USB Descriptors and Adapter Configuration from EEPROM after power-on initialization
- Provides optional serial interface: I^2C, SPI and UART
- Integrates on-chip voltage regulator and only requires a single 3.3V power supply
- 12MHz and 25MHz clock input from either crystal or oscillator source
- Integrates on-chip power-on reset circuit
- Small form factor with 64-pin LQFP (AX88772A) or 80-pin TQFP (AX88172A) RoHS compliant package
- Operating temperature range: 0˚C to +70˚C

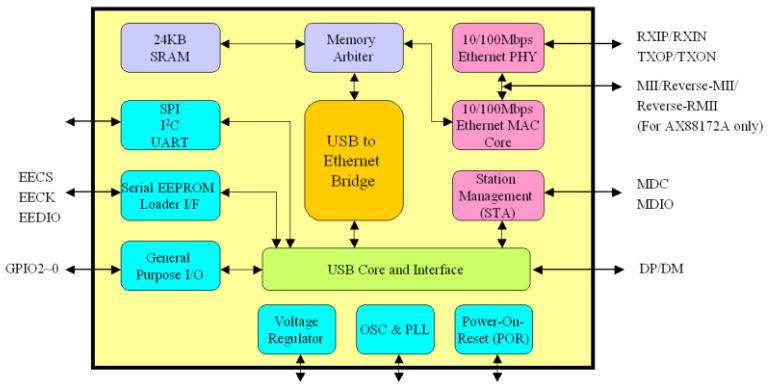
Product Description

The AX88x72A Low-pin-count USB 2.0 to 10/100M Fast Ethernet controller is a high performance and highly integrated ASIC which enables a low cost, small form factor and simple plug-and-play Fast Ethernet network connection capability for desktops, notebook PC's, UMPC's, cradles/port replicators/docking stations, game consoles, digital-home appliances and any embedded system using a standard USB port.

The AX88x72A features a USB interface to communicate with a USB Host Controller and is compliant with USB specification V1.1 and V2.0. The AX88x72A implements 10/100Mbps Ethernet LAN function based on IEEE802.3 and IEEE802.3u standards with 24KB of embedded SRAM for packet buffering. In addition, it integrates an on-chip 10/100Mbps Ethernet PHY, simplifying system design.

The AX88172A provides an optional External Media Interface (EMI) for an external PHY or an external MAC depending on different application purposes. The EMI can be a media-independent interface (MII) for implementing 100Base-FX Ethernet or HomePNA functions. The EMI can also be a Reverse-MII or Reverse Reduced-MII (Reverse-RMII) for glueless MAC-to-MAC connections to any MCU with Ethernet MAC MII or RMII interface. In addition, the EMI can be configured to Dual-PHY mode allowing the AX88172A to act as an Ethernet PHY or USB 2.0 PHY for external MAC devices that need Ethernet and USB interfaces in their system applications. Optional serial interfaces such as I^2C, SPI and UART are provided as a control channel from the USB Host Controller to communicate with the external MCU chip.

Block Diagram



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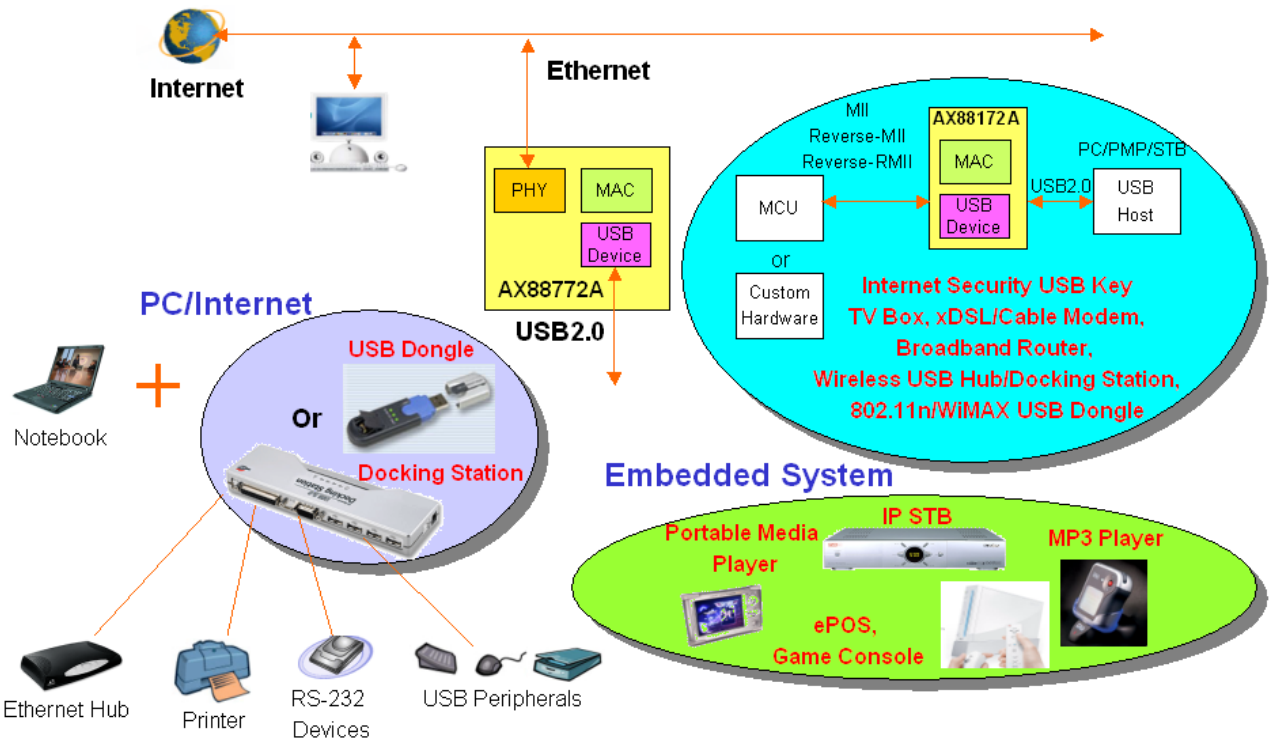
Application Diagram



High-speed USB-to-LAN Applications