USB 3.2 Gen1 to Gigabit Ethernet Controller

Document No: AX88179B/V1.06/09/23/26

Features

- **Single chip USB 3.2 Gen 1 to Gigabit Ethernet Controller with Integrated 10M/100M/1000M Ethernet PHY**
- **USB Device Controller**
  - Integrates on-chip USB Type-C 3.2 Gen1 PHY and controller compliant to USB Spec 3.2 Gen 1, 2.0 and 1.1
  - Supports all USB 3.2 Gen 1 power saving modes (U0, U1, U2, and U3)
  - Supports USB Super/High/Full Speed modes with Bus-power or Self-power device
- **Gigabit Ethernet Controller**
  - Integrates 10M/100M/1000M Gigabit Ethernet MAC/PHY, compliant to IEEE 802.3, 802.3u and 802.3ab
  - Supports CDC-NCM, CDC-ECM
  - Supports IEEE 802.3az (Energy Efficient Ethernet, EEE)
  - Supports AUTO-MDIX, flow control (IEEE 802.3 Annex.31B)
  - Supports IPv4/IPv6 Packet Checksum Offload Engine (COE)
  - Supports TCP Large Send Offload V1/V2
  - Supports up to 9K Jumbo Frame
  - Supports IEEE 802.1Q VLAN tagging and 4096 VLAN ID filtering; received VLAN tag (4 bytes) can be stripped off or preserved
  - Supports IEEE 802.1P Layer 2 Priority Encoding and Decoding
  - Supports manageability L2 filter
  - Supports TCO filter, L3/L4 IP/Port filter
  - Supports Second DA RX filter with bit mask
- **Wake-on-LAN Functions**
  - Supports suspend mode and remote wakeup via link-change, Magic Packet, Microsoft wakeup frame and external wakeup pin
  - Supports Bonjour Wake-on-Demand
  - Supports Wakeup Packet Indication
  - Supports Microsoft Modern Standby
- **Advanced Power Management Features**
  - Supports power management offload (ARP & NS)
  - Supports ECMA-393 ProxZzzy® for sleeping hosts
- **PTP (Precision Time Protocol)**
  - Supports IEEE 1588v2 and 802.1AS
- **Supports Windows 11/10/8.x, Linux/Android /Chrome OS, Nintendo Switch in-box drivers, and macOS/Linux native CDC-NCM driver for driverless, Plug & Play**
- **Supports embedded eFuse for die identifier and store the USB Device Descriptors, Node-ID, etc.**
- **Supports SPI Flash for firmware customization**
- **Single 20 MHz crystal clock source**
- **Integrates on-chip power-on reset circuit**
- **40-pin QFN, 5x5 mm package**
- **Operating Temperature Range: 0 to +70°C or -40 to +85°**

Target Applications

- Notebook/Laptop Onboard LAN
- USB Ethernet Dongle for Ultrabook /Table/Smart Phone/etc.
- Docking Station, POS/PDA Cradle
- IP STB, Smart Camera, Smart TV Box
- Game Console
- 5G/LTE Router/Gateway

ASIX Electronics Corporation
4F, No.8, Hsin Ann Rd.,
Hsinchu Science Park,
Hsinchu, Taiwan 30078

Released Date: 09/23/2026
TEL: +886-3-579-9500
FAX: +886-3-579-9558
https://www.asix.com.tw/

Typical Applications Diagram

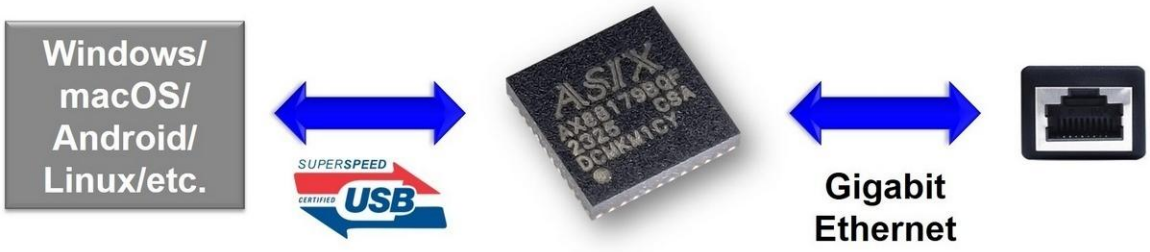


Figure 0-1: AX88179B Typical Applications Diagram

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

DISCLAIMER

No part of this document may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, for any purpose, without the express written permission of ASIX. ASIX may make changes to the product specifications and descriptions in this document at any time, without notice.

ASIX provides this document “as is” without warranty of any kind, either expressed or implied, including without limitation warranties of merchantability, fitness for a particular purpose, and non-infringement.

Designers must not rely on the absence or characteristics of any features or registers marked “reserved”, “undefined” or “NC”. ASIX reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. Always contact ASIX to get the latest document before starting a design of ASIX products.

TRADEMARKS

ASIX, the ASIX logo are registered trademarks of ASIX Electronics Corporation. All other trademarks are the property of their respective owners.

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

Table of Contents

1 INTRODUCTION 6
1.1 GENERAL DESCRIPTION 6
1.2 BLOCK DIAGRAM 6
1.3 PINOUT DIAGRAM 7
1.4 SIGNAL DESCRIPTION 8
1.4.1 USB Interface 8
1.4.2 Clock 8
1.4.3 GPHY MDI 8
1.4.4 Misc Pin 9
1.4.5 Power and Ground Pin 9
2 FUNCTION DESCRIPTION 10
2.1 CLOCKS/RESETS 10
2.2 USB CORE AND INTERFACES 10
2.3 10/100/1000M ETHERNET PHY 10
2.4 ENERGY EFFICIENT ETHERNET (EEE) 10
2.5 CHECKSUM OFFLOAD ENGINE (COE) 11
2.6 USB TO ETHERNET BRIDGE 11
2.7 EFUSE 11
2.8 GENERAL PURPOSE I/O AND LED 11
3 SPI/EFUSE MEMORY 12
3.1 SPI/EFUSE MEMORY 12
4 USB CONFIGURATION STRUCTURE 12
4.1 USB CONFIGURATION 12
4.2 USB INTERFACE 12
4.3 USB ENDPOINTS 12
5 ELECTRICAL SPECIFICATIONS 13
5.1 DC CHARACTERISTICS 13
5.1.1 Absolute Maximum Ratings 13
5.1.2 Recommended Operating Condition 13
5.1.3 DC Characteristics of 3.3V I/O Pins 14
5.2 POWER CONSUMPTION 15
5.3 POWER-ON-RESET (POR) SPECIFICATION 17
5.4 POWER–UP SEQUENCE 18
5.5 AC TIMING CHARACTERISTICS 19
5.5.1 SPI Timing 19
5.5.2 Clock Timing 20
5.5.3 Reset Timing 20
6 PACKAGE INFORMATION 21
7 ORDERING INFORMATION 22
8 REVISION HISTORY 23

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

List of Figures

FIGURE 0-1: AX88179B TYPICAL APPLICATIONS DIAGRAM 2
FIGURE 1-1: AX88179B BLOCK DIAGRAM 6
FIGURE 1-2: AX88179B PINOUT DIAGRAM 7
FIGURE 5-1: POWER ON RESET (POR) TIMING DIAGRAM 17
FIGURE 5-2: POWER-UP SEQUENCE TIMING DIAGRAM 18
FIGURE 5-3: SPI TIMING 19
FIGURE 5-4: CLOCK TIMING DIAGRAM 20

List of Tables

TABLE 1-1: USB INTERFACE PIN DESCRIPTION 8
TABLE 1-2: CLOCK PIN DESCRIPTION 8
TABLE 1-3: GPHY MDI PIN DESCRIPTION 8
TABLE 1-4: MISC PIN DESCRIPTION 9
TABLE 1-5: POWER AND GROUND PIN DESCRIPTION 9
TABLE 5-1: AX88179B POWER CONSUMPTION 15
TABLE 5-2: THERMAL CHARACTERISTICS 16
TABLE 5-3: POWER ON RESET (POR) TIMING TABLE 17
TABLE 5-4: POWER-UP SEQUENCE TIMING TABLE 18
TABLE 5-5: SPI TIMING TABLE 19
TABLE 5-6: CLOCK TIMING TABLE 20
TABLE 5-7: RESET TIMING TABLE 20

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

1 Introduction

1.1 General Description

The AX88179B USB 3.2 Gen1 to 10/100/1000M Gigabit Ethernet controller is a high performance and highly integrated ASIC which enables low cost, small form factor, and simple plug-and-play Gigabit Ethernet network connection capability for desktops, notebook PC's, Ultrabook's, docking stations, game consoles, digital-home appliances, and any embedded system using a standard USB port.

The AX88179B features a USB interface to communicate with a USB Host Controller and is compliant with USB specification V3.2 Gen1, V2.0, and V1.1. It implements a 10/100/1000Mbps Ethernet LAN function based on IEEE802.3, IEEE802.3u, and IEEE802.3ab standards with embedded SRAMs for packet buffering. And, it also integrates an on-chip 10/100/1000Mbps EEE-compliant Ethernet PHY to simplify system design.

1.2 Block Diagram

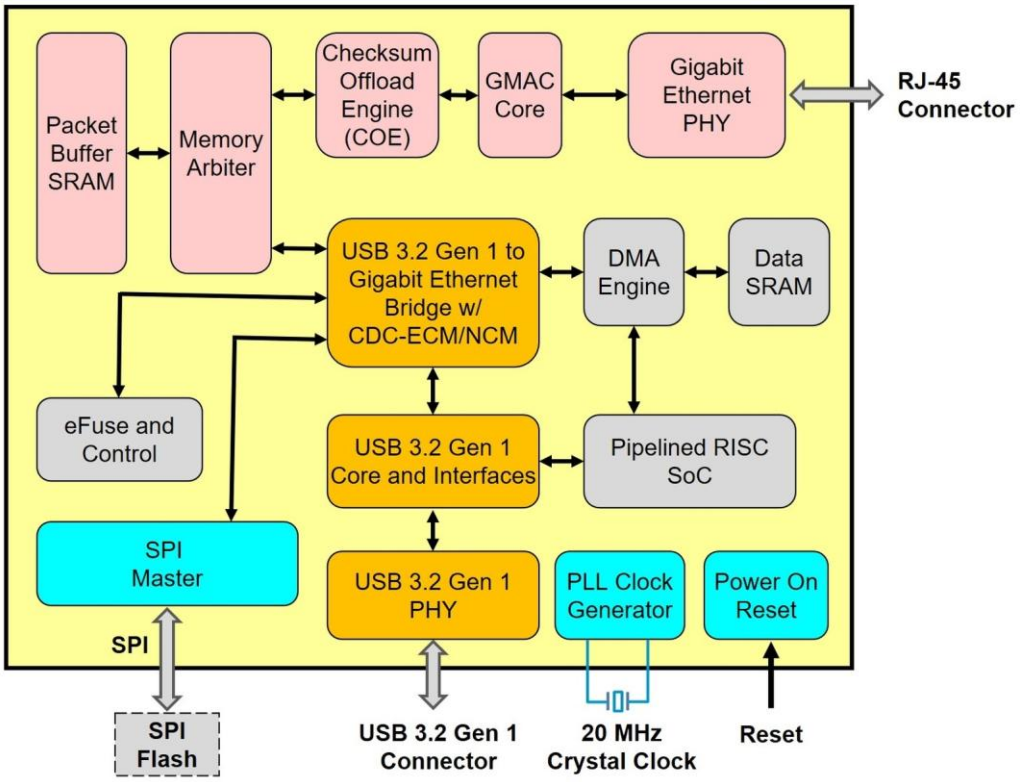


Figure 1-1: AX88179B Block Diagram

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

1.3 Pinout Diagram

AX88179B is housed in a 40-pin E-PAD QFN package.

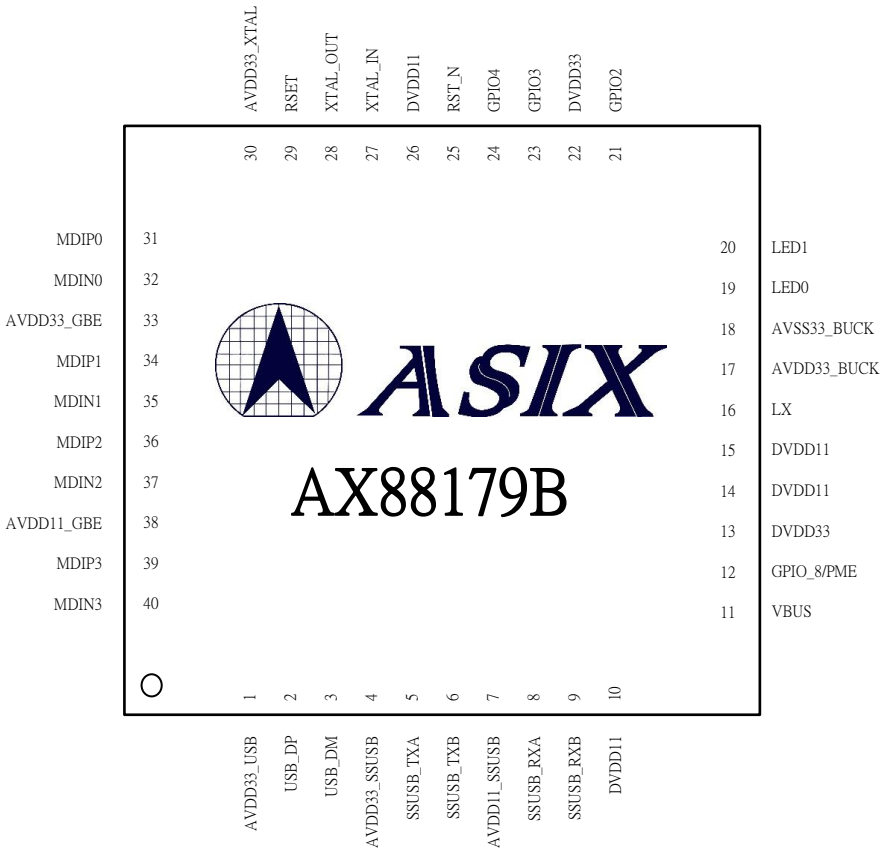


Figure 1-2: AX88179B Pinout Diagram

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

1.4 Signal Description

Following abbreviations are used in "Type" column of below pin description tables. Note that some I/O pins with multiple signal definitions on the same pin may have different attributes in "Type" column for different signal definition.

AB Analog Bi-directional I/O
AI Analog Input
AO Analog Output
B3 Bi-directional I/O, 3.3V
I3 Input, 3.3V
O3 Output, 3.3V
PU Internal Pull-Up (75K)
PD Internal Pull-Down (75K)
P Power/Ground pin
S Schmitt Trigger
T Tri-state
4m 4mA driving strength
8m 8mA driving strength

1.4.1 USB Interface

Pin Name	Type	Pin No	Pin Description
USB_DP	AB	2	USB 2.0 data differential pair positive pin.
USB_DM	AB	3	USB 2.0 data differential pair negative pin.
SSUSB_TXA	AO	5	USB 3.2 Gen 1 TX- differential pair pin A.
SSUSB_TXB	AO	6	USB 3.2 Gen 1 TX+ differential pair pin B.
SSUSB_RXA	AI	8	USB 3.2 Gen 1 RX- differential pair pin A.
SSUSB_RXB	AI	9	USB 3.2 Gen 1 RX+ differential pair pin B.

Table 1-1: USB Interface Pin Description

1.4.2 Clock

Pin Name	Type	Pin No	Pin Description
XTAL_IN	I3	27	20Mhz crystal clock input.
XTAL_OUT	O3	28	20Mhz crystal clock output.

Table 1-2: Clock Pin Description

1.4.3 GPHY MDI

Pin Name	Type	Pin No	Pin Description
MDIP0	AB	31	MDI pair 0 positive pin
MDIN0	AB	32	MDI pair 0 negative pin
MDIP1	AB	34	MDI pair 1 positive pin
MDIN1	AB	35	MDI pair 1 negative pin
MDIP2	AB	36	MDI pair 2 positive pin
MDIN2	AB	37	MDI pair 2 negative pin
MDIP3	AB	39	MDI pair 3 positive pin
MDIN3	AB	40	MDI pair 3 negative pin

Table 1-3: GPHY MDI Pin Description

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

1.4.4 Misc Pin

Pin Name	Type	Pin No	Pin Description
RSET	AB	29	External Reference Resistor (24 KΩ, 1%) Connect resistor to Analog GND.
VBUS	I3/S	11	VBUS signal of USB.
RST_N	I3/S/PU	25	Reset signal. Active low
GPIO_2	B3/S	21	Clock pin of SPI.
GPIO_3	B3/S	23	SPI data I/O pin if GPIO_4 pulled up.
GPIO_4	B3/S	24	If pulled up, CS pin of SPI
GPIO_8/PME*	B3/S/PU	12	PME pin for power management, always pull up this pin.
LED_0	B3	19	Programmable LED_0 indication
LED_1	B3	20	Programmable LED_1 indication

*: It is a multi-function pin. The default is an external wakeup pin. Active low. PME pin needs to set by tool.

Table 1-4: Misc Pin Description

1.4.5 Power and Ground Pin

Pin Name	Type	Pin No	Pin Description
AVDD33_USB	P	1	3.3V Analog Power Input of USB.
AVDD33_SSUSB	P	4	3.3V Analog Power Input of SS USB.
AVDD11_SSUSB	P	7	1.1V Analog Power Input of SS USB.
DVDD11	P	10	1.1V Digital Power.
DVDD33	P	13	3.3V I/O Power.
DVDD11	P	14	1.1V Digital Power.
DVDD11	P	15	1.1V Digital Power.
LX	P	16	This 1.1V power pin drives external inductors for on-die BUCK.
AVDD33_BUCK	P	17	3.3V Analog Power for on-die BUCK.
AVSS33_BUCK	P	18	3.3V Analog Ground for on-die BUCK.
DVDD33	P	22	3.3V I/O Power.
DVDD11	P	26	1.1V Digital Power.
AVDD33_XTAL	P	30	3.3V Analog Power for crystal pad.
AVDD33_GBE	P	33	3.3V Analog Power for Ethernet PHY.
AVDD11_GBE	P	38	1.1V Analog Power for Ethernet PHY.

Table 1-5: Power and Ground Pin Description

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

2 Function Description

2.1 Clocks/Resets

The AX88179B integrates internal PLL oscillator for 20 MHz (20MHz ± 50PPM at room temperature), respectively, which allow the chip to operate cost effectively with just one single external 20 MHz crystal.

The external 20 MHz crystal, via pins XTAL_IN / XTAL_OUT, provides the reference clock to internal oscillation circuit to generate clock source for the embedded Ethernet PHY, embedded USB PHY, and base clock for ASIC use.

The AX88179B integrates an internal power-on-reset circuit, which can simplify the external reset circuitry on PCB design. The power-on-reset circuit generates a reset pulse to reset chip logic after 1.1V core power ramping up to 0.72V (typical threshold). The external hardware reset input pin, RST_N, is fed directly to the input of the power-on-reset circuit and can also be used as additional hardware reset source to reset the system logic. For more details on RST_N timing, please refer to the Reset timing section.

2.2 USB Core and Interfaces

The USB core and interfaces contain USB 3.2 Gen1/USB 2.0 transceiver interfaces (PIPE/UTMI) and USB 3.2 Gen1/USB 2.0 Device Controller.

The USB 3.2 Gen1/USB 2.0 transceiver (or PHY) processes USB 3.2 Gen1/2.0/1.1 Physical layer signals. And, The USB 3.2 Gen1/USB 2.0 Device Controller is interfacing with USB 3.2 Gen1/USB 2.0 transceiver by PIPE/UTMI buses and it processes packets of Link layer and protocol layer. Also, The USB 3.2 Gen1/USB 2.0 Device Controller contains Bulk IN and Bulk OUT buffers for handling Bulk transfer traffic and a FIFO for Interrupt IN transfers.

The USB core and interfaces are used to communicate with a USB host controller and is compliant with USB specification V3.2 Gen1, V2.0, and V1.1

2.3 10/100/1000M Ethernet PHY

The 10/100/1000M Ethernet PHY is compliant with 10Base-T, 100Base-TX, and 1000Base-T IEEE 802.3 standards. It provides all the necessary physical layer functions to transmit and receive Ethernet packets over CAT 5e UTP cable or CAT 3 UTP (10Mbps only) cable. It uses DSP technology and an Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Functions such as Crossover Detection & Auto-Correction (Auto-MDIX), polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented.

2.4 Energy Efficient Ethernet (EEE)

It supports IEEE 802.3az also known as Energy Efficient Ethernet (EEE). And also supports EEE specified a negotiation method to enable link partner to determine whether EEE is supported and to select the best set of parameters common to both devices. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled; however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

2.5 Checksum Offload Engine (COE)

The Checksum Offload Engine (COE) supports IPv4, IPv6, layer 4 (TCP, UDP, ICMP, ICMPv6 and IGMP) header processing functions and real time checksum calculation in hardware

The COE supports the following features in layer 3:

- IP header parsing, including IPv4 and IPv6
- IPv6 extension header and routing header type 0 supported
- IPv4 header checksum check and generation (There is no checksum field in IPv6 header)
- Detecting on RX direction for IP packets with error header checksum

The COE supports the following features in layer 4:

- TCP and UDP checksum check and generation for non-fragmented packet
- TCP Large Send Offload V2
- ICMP, ICMPv6 and IGMP message checksum check and generation for non-fragmented packet.

2.6 USB to Ethernet Bridge

The USB to Ethernet bridge block is responsible for converting Ethernet MAC frame into USB packets or vice-versa. This block supports proprietary burst transfer mechanism (US Patent Approval) to offload software burden and to offer very high packet transfer throughput over USB bus.

This USB to Ethernet bridge block not only co-work with “eFuse and Control”, “SPI Loader I/F”, and General Purpose I/Os and LEDs, but also handle USB Control transfers of Endpoint 0.

2.7 eFuse

The AX88179B integrated an eFuse which is allowed user to program USB descriptions (PID, VID, Serial numbers… ect) and some device information (MAC address). And ASIX advance data structures allow user to program this information for multiple times.

2.8 General Purpose I/O and LED

There are 3 general-purpose I/O pins for SPI flash and 2 LED pins for LED indication.

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

3 SPI/eFuse Memory

3.1 SPI/eFuse Memory

AX88179B supports integrated eFuse for MAC address, USB descriptor and several user specified information. It also supports optional external SPI flash for firmware customization. These non-violated memory supports advance data architecture for multiple times programming.

4 USB Configuration Structure

4.1 USB Configuration

The AX88179B supports 2 USB Configuration, 1 for AX88179B proprietary driver, 1 for CDC-ECM/NCM.

4.2 USB Interface

The AX88179B supports 1 interface.

4.3 USB Endpoints

The AX88179B supports following 4 endpoints:

Endpoint 0: Control endpoint. It is used for configuring the device. Please refer to the USB Standard Commands and USB Vendor Commands sections.
Endpoint 1: Interrupt endpoint. It is used for reporting network Link status. Please refer to the Interrupt Endpoint section.
Endpoint 2: Bulk IN endpoint. It is used for receiving Ethernet Packet.
Endpoint 3: Bulk OUT endpoint. It is used for transmitting Ethernet Packet.

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

5 Electrical Specifications

5.1 DC Characteristics

5.1.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
DVDD33 AVDD33_USB AVDD33_SSUSB AVDD33_BUCK AVDD33_XTAL AVDD33_GBE	3.3V Supply Voltage	-0.3	3.63	V
DVDD11 AVDD11_SSUSB AVDD11_GBE	1.1V Supply Voltage	-0.1	1.2	V

Note:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the optional sections of this datasheet. Exposure to absolute maximum rating condition for extended periods may affect device reliability.
2. The input and output negative voltage ratings may be exceeded if the input and output currents under ratings are observed.

5.1.2 Recommended Operating Condition

Symbol	Parameter		Min	Typ	Max	Units
AVDD33_USB	3.3V Analog Power Input of USB.		3.14	3.3	3.46	V
AVDD33_SSUSB	3.3V Analog Power Input of SS USB.		3.14	3.3	3.46	V
AVDD11_SSUSB	1.1V Analog Power Input of SS USB.		1.045	1.1	1.155	V
DVDD11	1.1V Digital Power.		1.045	1.1	1.155	V
DVDD33	3.3V I/O Power.		3.14	3.3	3.46	V
AVDD33_BUCK	3.3V Analog Power Input of BUCK.		3.14	3.3	3.46	V
AVDD33_XTAL	3.3V Analog Power Input of Crystal.		3.14	3.3	3.46	V
AVDD33_GBE	3.3V Analog Power Input of Ethernet PHY.		3.14	3.3	3.46	V
AVDD11_GBE	1.1V Analog Power Input of Ethernet PHY.		1.045	1.1	1.155	V
Tj	Maximum junction temperature		-	-	125	℃
Ta	Operating ambient temperature	AX88179BQF	0	-	70	℃
		AX88179BQI	-40	-	85	℃
T_{STG}	Storage temperature		-65	-	150	℃

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

5.1.3 DC Characteristics of 3.3V I/O Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DVDD33	Power supply of 3.3V I/O.	3.3V I/O	3.14	3.3	3.46	V
Vil	Input low voltage.	LVTTL	-	-	0.8	V
Vih	Input high voltage.		2.0	-	-	V
Vt-	Schmitt trigger negative going threshold voltage.	LVTTL	0.8	1.1	-	V
Vt+	Schmitt trigger positive going threshold voltage		-	1.6	2.0	V
Vol	Output low voltage.	Iol = 4 ~ 8mA	-	-	0.4	V
Voh	Output high voltage.	Ioh = 4 ~ 8mA	DVDD33 -0.4	-	-	V
Vopu (1)	Output pull-up voltage for 5V tolerant IO	With internal pull-up resistor	DVDD33 – 0.9	-	-	V
Rpu	Input pull-up resistance.		40	75	190	KΩ
Rpd	Input pull-down resistance.		40	75	190	KΩ
Iin	Input leakage current.	Vin = 3.3 or 0V	-	±6	-	μA
	Input leakage current with pull-up resistance.	Vin = 0 V	-	-45	-	μA
	Input leakage current with pull-down resistance.	Vin = DVDD33	-	45	-	μA

Note: This parameter indicates that the pull-up resistor for the I/O pins cannot reach DVDD33 DC level even without DC loading current.

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

5.2 Power Consumption

Symbol	Description	Conditions	Typ	Unit
I_{VDD11}	Current Consumption of 1.1V	Operating at Ethernet 1Gbps full duplex mode and USB Super Speed mode	104.3	mA
I_{VDD33}	Current Consumption of 3.3V		90.5	mA
I_{VDD11}	Current Consumption of 1.1V	Operating at Ethernet 100Mbps full duplex mode and USB Super Speed mode	73.4	mA
I_{VDD33}	Current Consumption of 3.3V		42.6	mA
I_{VDD11}	Current Consumption of 1.1V	Operating at Ethernet 100Mbps half duplex mode and USB Super Speed mode	73.3	mA
I_{VDD33}	Current Consumption of 3.3V		42.6	mA
I_{VDD11}	Current Consumption of 1.1V	Operating at Ethernet 10Mbps half duplex mode and USB Super Speed mode	63.5	mA
I_{VDD33}	Current Consumption of 3.3V		32.7	mA
I_{VDD11}	Current Consumption of 1.1V	Operating at Ethernet 1Gbps full duplex mode and USB High Speed mode	64	mA
I_{VDD33}	Current Consumption of 3.3V		90.1	mA
I_{VDD11}	Current Consumption of 1.1V	Operating at Ethernet 100Mbps full duplex mode and USB High Speed mode	34	mA
I_{VDD33}	Current Consumption of 3.3V		33.2	mA
I_{VDD11}	Current Consumption of 1.1V	Operating at Ethernet 100Mbps half duplex mode and USB Super Speed mode	33.8	mA
I_{VDD33}	Current Consumption of 3.3V		29.7	mA
I_{VDD11}	Current Consumption of 1.1V	Operating at Ethernet 10Mbps half duplex mode and USB High Speed mode	22.6	mA
I_{VDD33}	Current Consumption of 3.3V		38.5	mA
I_{VDD11}	Current Consumption of 1.1V	Operating at Ethernet 1Gbps full duplex mode and USB Full Speed mode	59.4	mA
I_{VDD33}	Current Consumption of 3.3V		75	mA
I_{VDD11}	Current Consumption of 1.1V	Operating at Ethernet 100Mbps full duplex mode and USB Full Speed mode	30.7	mA
I_{VDD33}	Current Consumption of 3.3V		31	mA
I_{VDD11}	Current Consumption of 1.1V	Operating at Ethernet 100Mbps half duplex mode and USB Full Speed mode	30.6	mA
I_{VDD33}	Current Consumption of 3.3V		26	mA
I_{VDD11}	Current Consumption of 1.1V	Operating at Ethernet 10Mbps half duplex mode and USB Full Speed mode	21.4	mA
I_{VDD33}	Current Consumption of 3.3V		23	mA
I_{VDD11}	Current Consumption of 1.1V	Ethernet unlink (Disable AutoDetach) and USB Super Speed mode	62.8	mA
I_{VDD33}	Current Consumption of 3.3V		31.2	mA
I_{VDD11}	Current Consumption of 1.1V	Ethernet unlink (Enable AutoDetach)	14.7	mA
I_{VDD33}	Current Consumption of 3.3V		7.3	mA
I_{VDD11}	Current Consumption of 1.1V	USB Suspend and Ethernet is 1Gbps: enable Remote WakeUp and disable WOLLP (WOL Low Power)	57.7	mA
I_{VDD33}	Current Consumption of 3.3V		70.6	mA
I_{VDD11}	Current Consumption of 1.1V	USB Suspend and enable Remote WakeUp and enable WOLLP to 10Mbps	19.4	mA
I_{VDD33}	Current Consumption of 3.3V		11.9	mA
I_{VDD11}	Current Consumption of 1.1V	Suspend and disable Remote WakeUp	0.8	mA
I_{VDD33}	Current Consumption of 3.3V		0	mA
.				
I_{VDD11}	Current Consumption of 1.1V	Operating at Ethernet 1Gbps mode and USB Super Speed mode (Ethernet linked in EEE)	58.8	mA
I_{VDD33}	Current Consumption of 3.3V		70.3	mA
I_{VDD11}	Current Consumption of 1.1V	Operating at Ethernet 1Gbps mode and USB Super Speed mode (Ethernet linked in non-EEE)	103	mA
I_{VDD33}	Current Consumption of 3.3V		89.5	mA
I_{VDD11}	Current Consumption of 1.1V	USB Suspend and enable Remote WakeUp (Ethernet linked in EEE 1Gbps mode)	19.2	mA
I_{VDD33}	Current Consumption of 3.3V		11.9	mA
I_{VDD11}	Current Consumption of 1.1V	USB Suspend and enable Remote WakeUp (Ethernet linked in non-EEE 1Gbps mode)	58.7	mA
I_{VDD33}	Current Consumption of 3.3V		69.9	mA
System				
I_{SYSTEM}	Power consumption of AX88179B full loading (chip only)	3.3V include 1.1V	137	mA
I_{SYSTEM}	Power consumption of AX88179B full loading (test board)	VBUS of 5.0V (Using Switching regulator with two ports:1.1/3.3V)	133	mA
$I_{SYSTEM\ (Suspend)}$	Power consumption of AX88179B (test board): Suspend and disable Remote WakeUp.	VBUS of 5.0V (Using Switching regulator with two ports:1.1/3.3V)	0.7	mA

Note: Above current value are typical values measured on AX88179B Test board.

Table 5-1: AX88179B Power Consumption

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

Symbol	Description	Condition	Min	Typ	Max	Unit
Θ_{JC}	Thermal resistance of junction to case		-	18.5	-	°C/W
Θ_{JA}	Thermal resistance of junction to ambient	Still Air	-	32.9	-	°C/W
Θ_{JB}	Thermal resistance of junction to board (PCB 4L)		-	9	-	°C/W
Ψ_{JT}	Junction to Top of the Package Characterization Parameter		-	0.67	-	°C/W

Table 5-2: Thermal Characteristics

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

5.3 Power-On-Reset (POR) Specification

Below figures and table show the two POR circuit spec during power ramp-up/down.

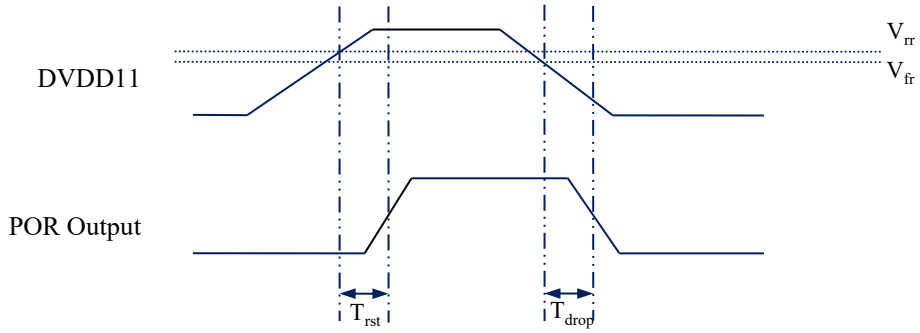


Figure 5-1: Power On Reset (POR) Timing Diagram

Symbol	Description	Conditions	Min.	Typ.	Max.	Units
DVDD11	Power supply voltage to be detected	-	1.045	1.1	1.155	V
V_{rr}	DVDD11 rise relax voltage	-	-	0.85	0.9	V
V_{fr}	DVDD11 fall release voltage	-	-	0.63	0.80	V
T_{rst}	Reset time after POR trigger up	DVDD11 slew rate = 1.0V / 1µs	1.8	2.5	4.8	µs
T_{drop}	Drop time of DVDD11 to reset	DVDD11 slew rate = 2.5V / 1µs	0.2	0.4	0.9	µs

Table 5-3: Power On Reset (POR) Timing Table

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

5.4 Power–up Sequence

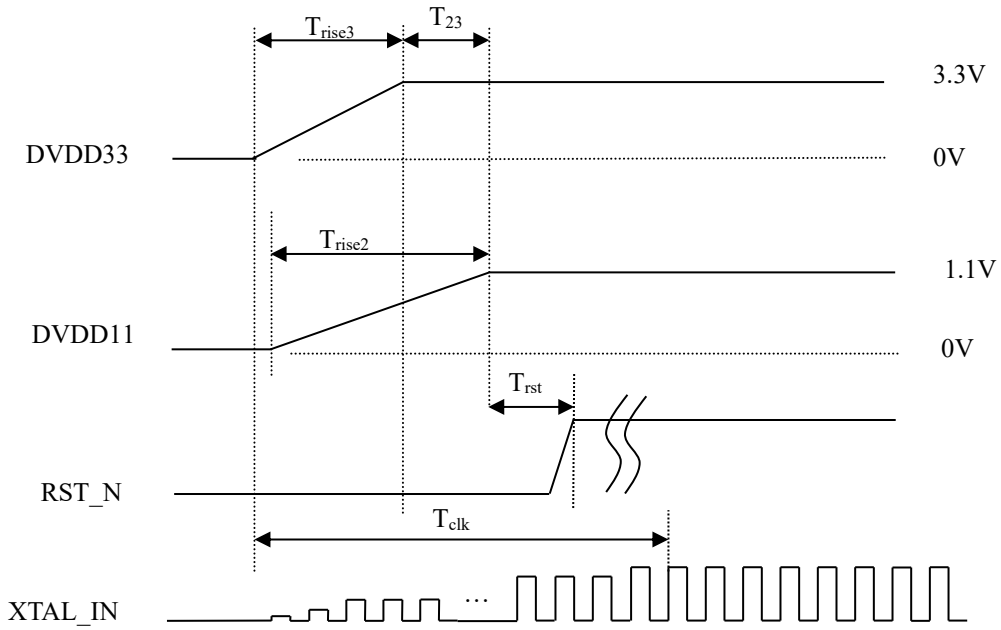


Figure 5-2: Power-up Sequence Timing Diagram

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{rise3}	3.3V power supply rise time.	From 0V to 3.3V.	-	1.15	-	ms
T_{rise2}	1.1V power supply rise time.	From 0V to 1.1V.	-	200	-	us
T_{23}	Interval between DVDD33 rising to 2.64V(80%) to DVDD11 rising to 0.88V(80%)		2	-	4	ms
T_{rst}	RST_N asserted low level interval.	From DVDD11 rising to 1.1V to RST_N going high.	-	1.15	-	ms
T_{clk}	20MHz crystal start-up time.	From DVDD33 rising to 3.3V to clock stable of 20MHz crystal.	-	-	20	ms

Note: The above typical timing data is measured from AX88179B test board.

Table 5-4: Power-up Sequence Timing Table

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

5.5 AC Timing Characteristics

5.5.1 SPI Timing

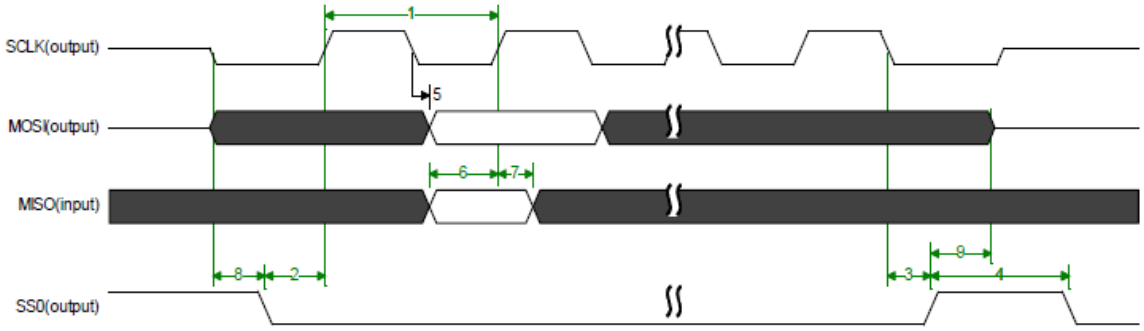


Figure 5-3: SPI Timing

Symbol	Parameter	Min	Typ	Max	Units
1	SCLK clock frequency	-	Fsys_clk (SPIBRR + 1) * 2		MHz
2	Setup time of SS to the first SCLK edge	-	0.5 * Tsclk	-	ns
3	Hold time of SS after the last SCLK edge	-	0.5 * Tsclk	-	ns
4	Minimum idle time between transfers (minimum SS high time)	-	((32 * SPIDT + 6) * Tsys_clk) + (0.5 * Tsclk)	-	ns
5	MOSI data valid time, after SCLK edge	-		1.53	ns
6	MISO data setup time before SCLK edge	5.98		-	ns
7	MISO data hold time after SCLK edge	0		-	ns
8, 9	Bus drive time before SS assertion and after SS de-assertion	-		0.5 * Tsclk	ns

Note 1: Fclk = 1/Tclk, where Tclk = ((SCL_HP + SCL_LP) * Tsys_clk).
Tsys_clk is 20MHz or 80MHz.

Table 5-5: SPI Timing Table

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

5.5.2 Clock Timing

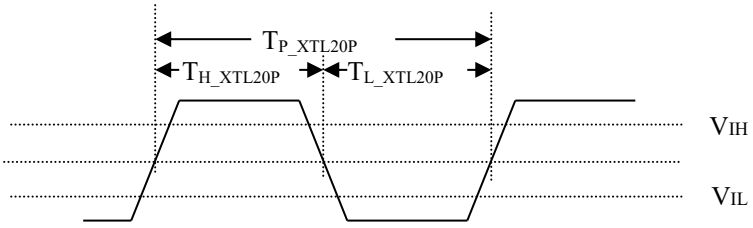
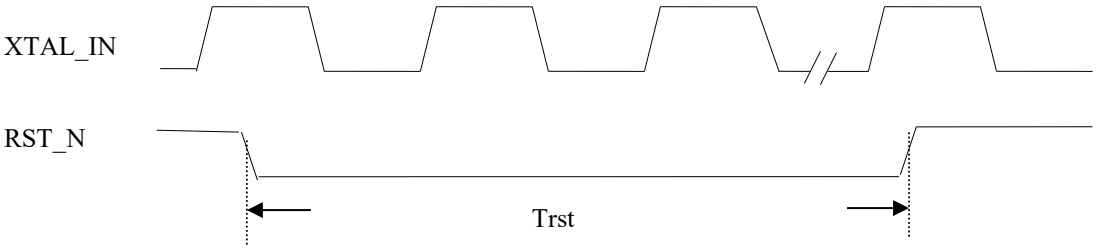


Figure 5-4: Clock Timing Diagram

Symbol	Parameter	Condition	Min	Typ		Max	Unit
T_{P_XTL20P}	XTL20P clock cycle time		-	50.0		-	ns
T_{H_XTL20P}	XTL20P clock high time		-	25.0		-	ns
T_{L_XTL20P}	XTL20P clock low time		-	25.0		-	ns

Table 5-6: Clock Timing Table

5.5.3 Reset Timing

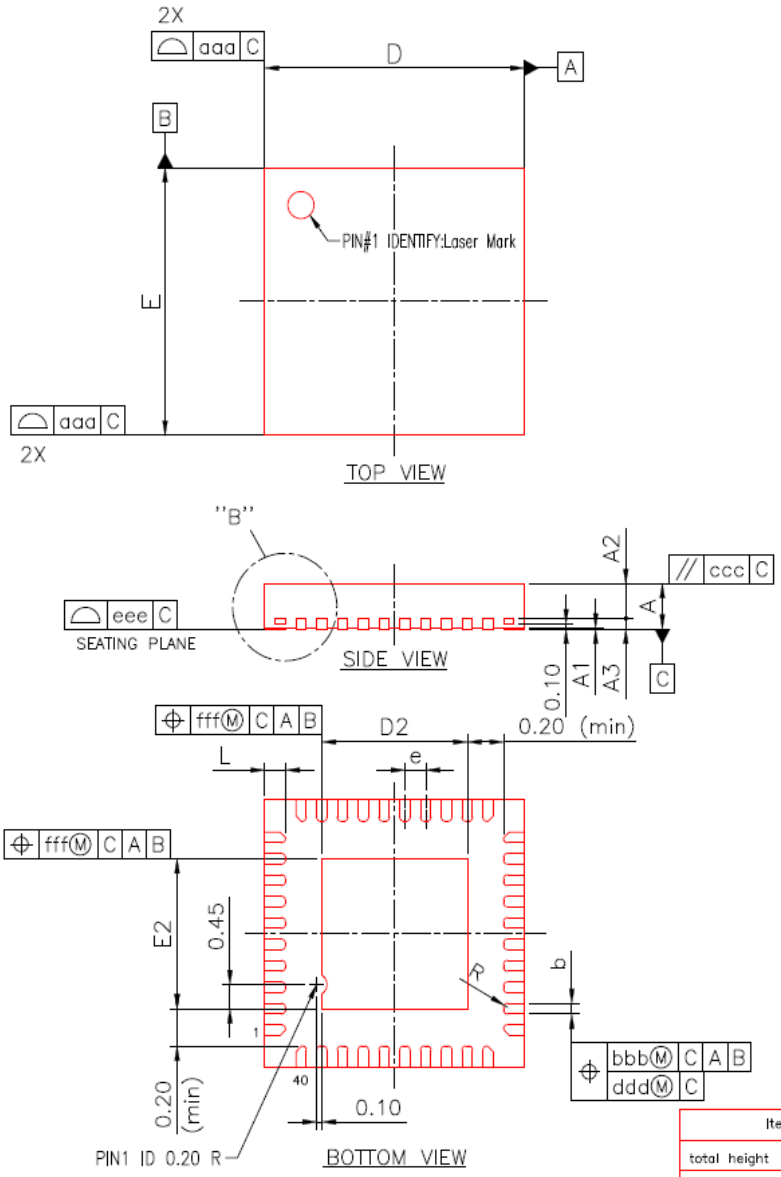


Symbol	Description	Min	Typ	Max	Unit
Trst	Reset pulse width after XTAL_IN is running	200	-	-	XTAL_IN clock cycle

Table 5-7: Reset Timing Table

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

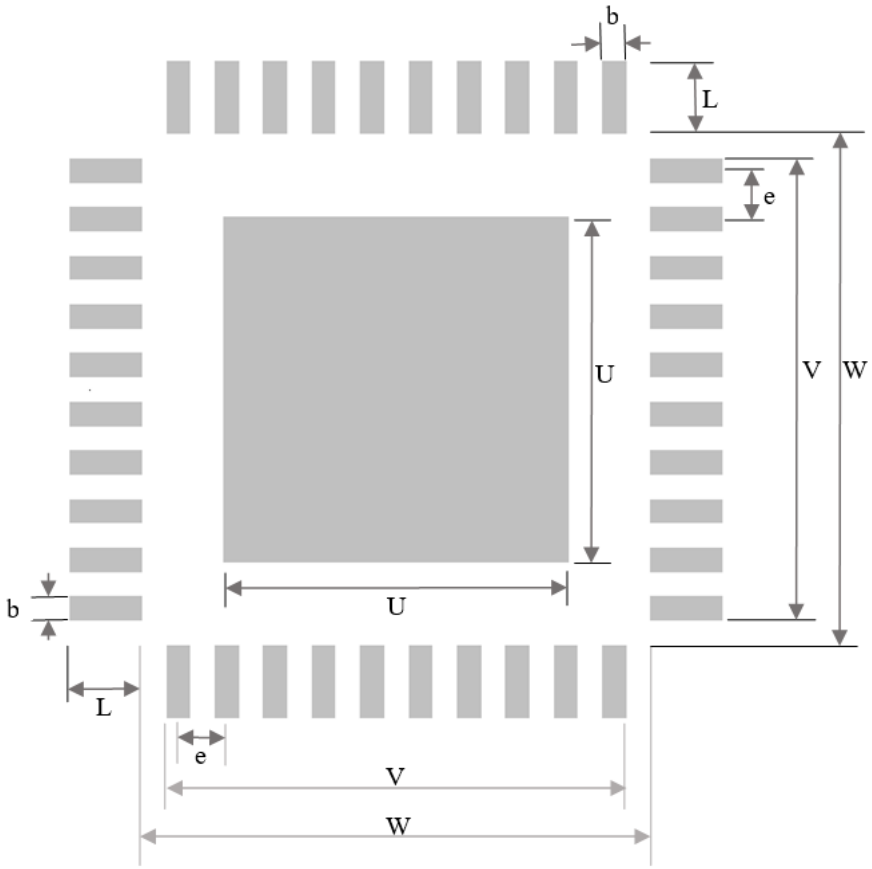
6 Package Information



Item		Symbol	MIN.	NOM.	MAX.
total height		A	0.80	0.85	0.90
stand off		A1	0.00	0.02	0.05
mold thickness		A2	0.60	0.65	0.70
leadframe thickness		A3	0.20 REF.		
lead width		b	0.15	0.20	0.25
package size	X	D	4.90	5.00	5.10
	Y	E	4.90	5.00	5.10
E-PAD size	X	D2	2.70	2.80	2.90
	Y	E2	2.70	2.80	2.90
lead length		L	0.30	0.40	0.50
lead pitch		e	0.40 bsc		
lead arc		R	0.075	---	---
Package profile of a surface		aaa	0.10		
Lead position		bbb	0.07		
Parallellism		ccc	0.10		
Lead position		ddd	0.05		
Lead profile of a surface		eee	0.08		
Epad position		fff	0.10		

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

Recommended PCB Footprint for 40-pin QFN 5x5 package



Symbol	Description	Typical Dimension
e	Lead pitch	0.40 mm
b	Pad width	0.20 mm
L	Pad length	0.60 mm
U	-	2.80 mm
V	-	3.80 mm
W	-	4.20 mm

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

7 Ordering Information

Part Number	Description
AX88179BQF	40-pin QFN lead Free package, Commercial temperature range: 0 to 70°C.
AX88179BQI	40-pin QFN lead Free package, Industrial temperature range: -40 to +85°C

8 Revision History

Revision	Date	Comments
V1.00	2023/10/13	Initial release.
V1.01	2023/12/04	Corrected signal definition in Section 1.4
V1.02	2024/01/17	Updated some description in Features page.
V1.03	2024/05/13	Added AX88179BQI information in Section 7.
V1.04	2025/02/11	Updated some description in Section 5.1.2
V1.05	2026/02/06	Updated some description in Section 5.4
V1.06	2026/09/23	Updated some description in Section 1.4.2, 2.1 and Table 5-4

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.

ASIX Electronics Corporation

4F, No.8, Hsin Ann RD., Hsinchu Science Park,
Hsinchu, Taiwan, R.O.C.

TEL: +886-3-5799500
FAX: +886-3-5799558

Email: support@asix.com.tw
Web: https://www.asix.com.tw

Copyright © 2023-2026 ASIX Electronics Corporation. All rights reserved.