AXM57104 Product Brief

Release Date: 06/13/2023

Quad Port TSN Gigabit Ethernet PCIe NIC Card

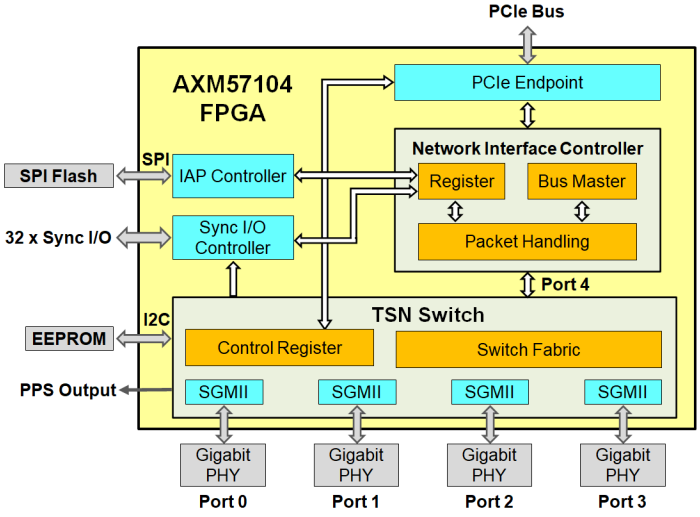
The AXM57104 is a 4-port TSN Gigabit Ethernet PCI Express network interface card, compliant to PCI Express base spec. v2.1 Gen1, which supports enhanced TSN functions included the timing and synchronization compliant to IEEE 802.1 AS-Rev/AS and IEEE 1588V2, the Credit-Based Shaper compliant to IEEE 802.1Qav, the Frame Preemption compliant to IEEE 802.1Qbu, the Time-Aware Shaper compliant to IEEE 802.1Qbv, and the Frame Replication and Elimination for Reliability compliant to IEEE 802.1CB. AXM57104 also supports 32 synchronous I/O pins, one Pulse Per Second (PPS) output, FPGA hard-core field upgradable via In Application Programming (IAP) for TSN standards evolution.

The AXM57104 is a cost-efficient PCIe to TSN solution for Industrial Internet of Things (IIoT) applications to enable TSN functions on industrial automation platforms, Fieldbus over TSN gateways and converge the non-real-time IT (Information Technology) network and real-time OT (Operation Technology) networks which work on different industrial Ethernet protocols such as EtherCAT/PROFINET/EtherNet IP/etc.

Key Features

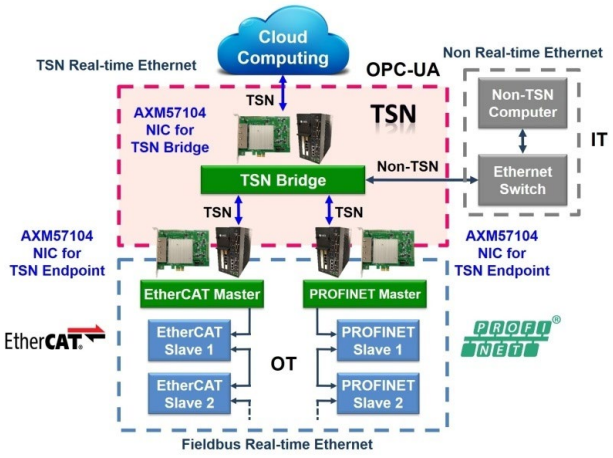
- **Compliant to PCI Express base spec. v2.1 Gen1**
- **PCIe Network Interface Controller (NIC)**
  - Gigabit Ethernet Network Interface Controller
  - Ethernet packet through Bus-Master DMA
  - Unicast/multicast/broadcast filters
  - Support Legacy and MSI interrupt
- **TSN Gigabit Ethernet Switch**
  - **IEEE 802.1AS-Rev/AS** and **IEEE 1588V2**: Timing and Synchronization
  - **IEEE 802.1Qav**: Forwarding and Queuing of Time Sensitive Streams (FQTSS) : Specifies Credit-Based Shaper (CBS)
  - **IEEE 802.1Qbu**: Frame Preemption
  - **IEEE 802.1Qbv**: Time-Aware Shaper (TAS)
  - **IEEE 802.1CB:** Frame Replication and Elimination for Reliability (FRER)
  - 4 Gigabit Ethernet SGMII interfaces
  - Support 8 priority queues
  - QoS according to the PCP bits (802.1p), or Ethertype
  - Port-based and 802.1Q tag-based VLANs
  - Support Independent VLAN Learning (IVL)
  - DSA (Distributed Switch Architecture) for frame tagging
  - Shared Dynamic and Static MAC Table (4096 entries), Automatic MAC addresses learning and ageing
  - Broadcast storm protection and multicast frames filtering
  - Per-port Frame rate limiting and Frame/Error counters
  - 32 Kbytes packet buffer per port
- **FPGA hard-core field upgradable via In Application Programming (IAP) for TSN standards evolution**
- **Support Board Support Package (BSP)**
- **32 Synchronous I/O pins and one I2C master**
- **One Pulse Per Second (PPS) output**
- **Support PCI Express x1 slot, Standard profile bracket**
- **Operating Temperature Range: -40 to +80˚C**

Block Diagram



Target Applications

- Enable TSN on Industrial Automation Platforms
- Fieldbus over TSN Gateway
- Converge IT & OT Networks



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