ZT483H/ZT485H/ZT488H/ZT489H/ZT490H/ZT491H
Low Power 5V 250Kbps/10Mbps 256-Fanout RS485 Transceivers
Datasheet

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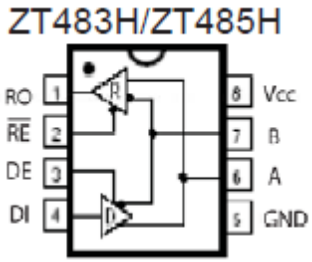
Features

- Meets or exceeds the requirements of ANSI Standard TIA/EIA-485-A and ISO 8482:1987(E) specifications for V_{CC} at +5V ±10%
- Low quiescent current – 0.4mA typ., 0.9mA max.
- Low shutdown current (where applicable) - 1μA typical, 10μA max.
- Guaranteed standard data rate 250Kbps or 10Mbps
- True Fail-Safe (Open, Short, Bus Idle) Receiver
- -7V to +12V common-mode input voltage range
- Half-Duplex mode configuration
- Allows up to 1/8 unit load (256 devices) on the same common bus
- Controlled driver output slew rate and receiver input filtering
- Active-high driver enable and active-low receiver enable
- ESD protection on bus terminals
  ±15KV Human Body Model (HBM)
- Alternative replacement for MAX308x, MAX1308x SN75HVD308x, SN65HVD308x
- Standard fanout driving 1 unit load (32 devices) on the ZT485E Series



General Description

The ZT485H series devices are 5V differential data line transceivers for RS485/RS422 communication that consist of one driver and one receiver with high level of ESD protection. They are designed for balanced transmission lines interface that meet ANSI standard TIA/EIA-485-A and ISO 8482:1987(E) specifications.

The ZT485H series devices spans out with half or full duplex, data rate guaranteed at 250K bit per second or 10Mbps, and allow one-eighth of an unit load that fan out 256 devices sharing a common bus. The I/Os are enhanced-electrostatic discharge (ESD) protected, exceeding ±15KV Human Body Model (HBM).

Applications

- RS422/RS485 communications
- Utility meters
- Industrial process control
- Building automation
- Level translators
- Transceivers for EMI-sensitive applications
- Routers and HUBs
- Industrial-controlled Local Area Networks
- Industrial PCs, embedded PCs and peripherals
- Industrial, security CATV and camera applications

• Product Selection Guide and Cross Reference

Part Number	Duplex	# 0f Tx/Rx	Data Rate (Mbps)	# of Tx/Rx on Bus	Slew Rate Limit	Rx Input Filtering	Low-Power Shutdown	Tx/Rx Enable	ESD on Tx/Rx	Package Types	Pin-to-Pin Cross Reference
ZT483H	Half	1/1	0.25	256	Yes	Yes	Yes	Yes	± 15KV	8-PDIP, 8-nSOIC	MAX3060, MAX3082E, SN65HVD3082E, SN75HVD3082E
ZT485H	Half	1/1	10	256	No	No	Yes	Yes	± 15KV	8-PDIP, 8-nSOIC	MAX3085E, MAX3088E, SN65HVD3085E
ZT488H	Full	1/1	0.25	256	Yes	Yes	No	No	± 15KV	8-PDIP, 8-nSOIC	MAX3084E
ZT489H	Full	1/1	0.25	256	Yes	Yes	Yes	Yes	± 15KV	14-PDIP, 14-nSOIC	MAX3083E
ZT490H	Full	1/1	10	256	No	No	No	No	± 15KV	8-PDIP, 8-nSOIC	MAX3087E
ZT491H	Full	1/1	10	256	No	No	Yes	Yes	± 15KV	14-PDIP, 14-nSOIC, 10-MSOP	MAX3086E

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Absolute Maximum Ratings

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Power Supply, (V_{CC}) .....–0.3V to +7.0V

Input Voltages

DI, DE, $\overline{RE}$ ..... –0.3V to (V_{CC} +0.3V)
Differential Input Voltage, (V_{ID}) ..... -12V to +12V
A, B (V_I) ..... -9V to +13V

Output Voltages

RO .....–0.3V to +6.0V
Y, Z (A & B on Half Duplex) .....-9V to +13.0V
Operating Temperature .....–40°C to +85°C
Storage Temperature .....–65°C to +150°C

Power Dissipation Per Package

8-pin PDIP (derate 9.09mW/°C above +70°C) 722mW
8-pin nSOIC (derate 6.14mW/°C above +70°C) 500mW
14-pin PDIP (derate 10.00mW/°C above +70°C) 800mW
14-pin nSOIC (derate 8.33mW/°C above +70°C) ….667mW
10-pin MSOP (derate 8.84mW/°C above +70°C)…..720mW

Storage Considerations

Storage in a low humidity environment is preferred. Large high density plastic packages are moisture sensitive and should be stored in Dry Vapor Barrier Bags. Prior to usage, the parts should remain bagged and stored below 40°C and 60%RH. If the parts are removed from the bag, they should be used within 168 hours or stored in an environment at or below 20%RH. If the above conditions cannot be followed, the parts should be baked for 12 hours at 125°C in order to remove moisture prior to soldering. ASIX ships product in Dry Vapor Barrier Bags with a humidity indicator card and desiccant pack. The humidity indicator should be below 30%RH. The MSL of this product is 3.

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1 DC Electrical Characteristics

Unless otherwise stated, V_{CC} = +5.0V, T_A = T_{min} to T_{max}, typical values apply at V_{CC} = +5.0V and T_A = 25°C.

Parameter	Condition	Min	Typ	Max	Units
Operating Voltage & Temperature					
Temperature	Industrial Grade	–40	25	85	°C
Vcc Voltage Range	V_{CC} = +5.0V	4.5	5	5.5	V
Supply Current					
Icc, Tx and Rx active	DI= Vcc /GND, DE= Vcc, $\overline{RE}$=GND, RS485 I/O=Open		400	900	μA
Icc, Tx active	DI= Vcc /GND, DE= Vcc, $\overline{RE}$= Vcc, RS485 I/O=Open		400	900	μA
Icc, Rx active	DI= Vcc /GND, DE=GND, $\overline{RE}$=GND, RS485 I/O=Open		400	900	μA
I_{SD}, Shutdown Current (ZT483H, ZT485H, ZT489H and ZT491H Only)	DI= Vcc /GND, DE = GND, $\overline{RE}$ = Vcc, RS485 I/O=Open		1	10	μA
TTL LOGIC Input, Driver					
Input Threshold Low, V_{IL}	Vcc = +5.0V, DE, DI, and $\overline{RE}$			0.8	V
Input Threshold High, V_{IH}	Vcc = +5.0V, DE, DI, and $\overline{RE}$	2			V
TTL LOGIC Output, Receiver					
Output Voltage Low, V_{OL}	I_{OUT} = +4mA, Input Differential Voltage = 200mV			0.4	V
Output Voltage High, V_{OH}	I_{OUT} = –4mA, Input Differential Voltage = 200mV	3.5			V
Output Leakage Current	Receiver Outputs Disabled, V_{OUT} = 0.4V to 2.4V			±1	μA
Short Circuit Current	V_{OUT} = 0V to Vcc			±95	mA
Receiver Input					
Input Current	DE = 0V, Vcc = 0V to 5.5V, V_{IN} = +12V			125	uA
	DE = 0V, Vcc = 0V to 5.5V, V_{IN} = –7V			-75	uA
Differential Threshold Voltage, V_{TH}	V_{CM} = 0V, Vcc =+5.0V, T_A=25°C	–0.2		0.2	V
Input Hysteresis	V_{CM} = 0V		20		mV
Input Resistance, R_{IN}	V_{CM} = -7V to +12V	96			KΩ
Transmitter Output					
Differential Output Voltage, V_{OD1}	No Load			5	V
Differential Output Voltage, V_{OD2}	With R_L = 50Ω, Refer to Figure 1. (RS422)	2			V
	With R_L = 27Ω, Refer to Figure 1. (RS485)	1.5		5	V
Driver Common Mode Output, V_{OC}	With R_L = 27Ω or 50Ω. C_L = 50pF. Refer to Figure 3.			3	V
Change in Voltage Magnitude for Differential States, ΔV_{OD}	Differential Output Voltage, with R_L = 27Ω or 50Ω, C_L = 50pF Refer to Figure 1			0.2	V
Change in Voltage Magnitude for Common Mode States, ΔV_{OC}	Common-Mode Output Voltage, with R_L = 60Ω/375Ω/375Ω. Refer to Figure 2.			0.2	V
Transmitter Short-Circuit Current	V_{OUT} = -7V to +12V. Refer to Figure 7.	-250		250	mA

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2 AC Electrical Characteristics (ZT485H, ZT490H, ZT491H)

Unless otherwise stated, V_{CC} = +5.0V, T_A = T_{min} to T_{max}, typical values apply at V_{CC} = +5.0V and T_A = 25°C.

Parameter	Condition	Min	Typ	Max	Units
Transmitter Timing					
Transmitter Propagation t_{PLH}	R_{DIFF} = 54Ω, C_L = 50pF. Refer to Figure 4.		35	60	ns
Transmitter Propagation t_{PHL}	R_{DIFF} = 54Ω, C_L = 50pF. Refer to Figure 4.		35	60	ns
Transmitter Output Skew t_{SK}	$\|t_{PLH} - t_{PHL}\|$		3	10	ns
Transmitter Rise/Fall Time	tr, tf, R_{DIFF} = 54Ω, C_L = 50pF. Refer to Figure 4.		15	25	ns
Transmitter Output Enable	To Output HIGH, C_L = 50pF, R_L = 110Ω. Refer to Figure 5.		50		ns
	To Output LOW, C_L = 50pF, R_L = 110Ω. Refer to Figure 6.		50		ns
Transmitter Output Disable	From Output HIGH, C_L = 50pF, R_L = 110Ω. Refer to Figure 5.		50		ns
	From Output LOW, C_L = 50pF, R_L = 110Ω. Refer to Figure 6.		50		ns
Receiver Timing					
Receiver Propagation t_{PLH}	C_L = 15pF, Refer to Figure 9.		50	150	ns
Receiver Propagation t_{PHL}	C_L = 15pF, Refer to Figure 9.		50	150	ns
Differential Receiver Skew t_{SK}	$\|t_{PLH} - t_{PHL}\|$		10		ns
Receiver Output Enable	To Output HIGH, C_L = 15pF. Refer to Figure 10.		50		ns
	To Output LOW, C_L = 15pF. Refer to Figure 11.		50		ns
Receiver Output Disable	From Output HIGH, C_L = 15pF. Refer to Figure 10.		50		ns
	From Output LOW, C_L = 15pF. Refer to Figure 11.		50		ns
Shutdown Timing (ZT485H and ZT491H ONLY)					
Time to Shutdown, t_{SHDN}			50	600	ns
Transmitter Enable from SHUTDOWN to Output HIGH	C_L = 50pF, R_L = 110Ω. Refer to Figure 5.		200		ns
Transmitter Enable from SHUTDOWN to Output LOW	C_L = 50pF, R_L = 110Ω. Refer to Figure 6.		200		ns
Receiver Enable from SHUTDOWN to Output HIGH	C_L = 15pF, R_L = 1KΩ. Refer to Figure 11.		200		ns
Receiver Enable from SHUTDOWN to Output LOW	C_L = 15pF, R_L = 1KΩ. Refer to Figure 11.		200		ns
Transceiver Throughput					
Maximum Data Rate	R_L = 54Ω, C_L = 50pF, T_A = 25°C.	10			Mbps
ESD Tolerance					
ESD HBM	RS485 Inputs and Outputs		±15		KV
ESD HBM (1)	All Pins		±4		KV

(1) Tested in accordance with JEDEC Standard 22, Test Method A114-A and IEC 60749-26

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3 AC Electrical Characteristics (ZT483H, ZT488H and ZT489H)

Unless otherwise stated, V_{CC} = +5.0V, T_A = T_{min} to T_{max}, typical values apply at V_{CC} = +5.0V and T_A = 25°C.

Parameter	Condition	Min	Typ	Max	Units
Transmitter Timing					
Transmitter Propagation t_{PLH}	R_{DIFF} = 54Ω, C_L = 50pF. Refer to Figure 4.	250	800	2000	ns
Transmitter Propagation t_{PHL}	R_{DIFF} = 54Ω, C_L = 50pF. Refer to Figure 4.	250	800	2000	ns
Transmitter Output Skew t_{SK}	$\|t_{PLH} - t_{PHL}\|$		20	800	ns
Transmitter Rise/Fall Time	tr, tf, R_{DIFF} = 54Ω, C_L = 50pF. Refer to Figure 4.	250		2000	ns
Transmitter Output Enable	To Output HIGH, C_L = 50pF, R_L = 110Ω. Refer to Figure 5.		100		ns
	To Output LOW, C_L = 50pF, R_L = 110Ω. Refer to Figure 6.		100		ns
Transmitter Output Disable	From Output HIGH, C_L = 50pF, R_L = 110Ω. Refer to Figure 5.		100		ns
	From Output LOW, C_L = 50pF, R_L = 110Ω. Refer to Figure 6.		100		ns
Receiver Timing					
Receiver Propagation t_{PLH}	C_L = 15pF, Refer to Figure 9.			2000	ns
Receiver Propagation t_{PHL}	C_L = 15pF, Refer to Figure 9.			2000	ns
Differential Receiver Skew t_{SK}	$\|t_{PLH} - t_{PHL}\|$		10		ns
Receiver Output Enable	To Output HIGH, C_L = 15pF. Refer to Figure 10.		100		ns
	To Output LOW, C_L = 15pF. Refer to Figure 11.		100		ns
Receiver Output Disable	From Output HIGH, C_L = 15pF. Refer to Figure 10.		100		ns
	From Output LOW, C_L = 15pF. Refer to Figure 11.		100		ns
Shutdown Timing (ZT483H and ZT489H ONLY)					
Time to Shutdown, t_{SHDN}			50	600	ns
Transmitter Enable from SHUTDOWN to Output HIGH	C_L = 50pF, R_L = 110Ω. Refer to Figure 5.		200		ns
Transmitter Enable from SHUTDOWN to Output LOW	C_L = 50pF, R_L = 110Ω. Refer to Figure 6.		200		ns
Receiver Enable from SHUTDOWN to Output HIGH	C_L = 15pF, R_L = 1KΩ. Refer to Figure 11.		200		ns
Receiver Enable from SHUTDOWN to Output LOW	C_L = 15pF, R_L = 1KΩ. Refer to Figure 11.		200		ns
Transceiver Throughput					
Maximum Data Rate	R_L = 54Ω, C_L = 50pF, T_A = 25°C.	0.25			Mbps
ESD Tolerance					
ESD HBM	RS485 Inputs and Outputs		±15		KV
ESD HBM (1)	All Pins		±4		KV

(1) Tested in accordance with JEDEC Standard 22, Test Method A114-A and IEC 60749-26

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4 Pin Description

Pin Numbers				Pin Name	Pin Description
Half Duplex	Full Duplex				
ZT483H	ZT488H	ZT489H	ZT491HLEEU (10-PIN MSOP)		
ZT485H	ZT490H	ZT491H			
1	2	2	1	RO	Receiver Output. If A>B by 200mV, then RO = HIGH; If A<B by 200mV, then RO = LOW
2	n/a	3	2	$\overline{RE}$	Receiver Output Enable Low active input RO is high-Z when $\overline{RE}$ = HIGH
3	n/a	4	3	DE	Driver Output Enable. The transmitter outputs, Y and Z, are enabled when DE = HIGH. The outputs are high-Z when DE = LOW
4	3	5	4	DI	Driver Input. A low on DI forces output Y low and output Z high. A high on DI will bring output Y high and output Z low
5	4	6, 7	5	GND	Analog Ground
n/a	5	9	6	Y	Non-inverting transmitter output
n/a	6	10	7	Z	Inverting transmitter output
6	n/a	n/a	n/a	A	Non-inverting transmitter output and non-inverting receiver input.
n/a	8	12	9	A	Non-inverting receiver input.
7	n/a	n/a	n/a	B	Inverting transmitter output and inverting receiver input.
n/a	7	11	8	B	Inverting receiver input
8	1	14	10	VCC	Power Supply Input, 5V ±10%
n/a	n/a	1, 8, 13	n/a	NC	No Connect, Not internally connected.

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5 Circuit Description

The ZT4xxH family are low-power transceivers for RS-485 and RS-422 communications. The RS-485 standard is ideal for multi-drop applications and for long-distance interfaces. The TIA/EIA-485 specification allows up to 256 drivers and 256 receivers to be connected to a data bus, making it an ideal choice for multi-drop applications. RS-485 transceivers are equipped with a wide (-7V to +12V) common mode range to accommodate ground potential differences since the cabling can be as long as 4,000 feet. As RS-485 is a differential interface, data is virtually immune to noise in the transmission line.

The ZT483H, ZT488H, and ZT489H are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables.

RS-485 Transmitters

Each device in the ZT4xxH family contains a differential output line transmitter that can drive voltage into multiple loads on a terminated two-wire pair, and a receiver that accepts a differential voltage down to 200mV. The transmitter's differential output can comply with RS-485 and also RS-422 standards. The typical voltage output swing with no load is 0V to Vcc. With worst case loading of 54 ohms across the differential outputs, the drivers can maintain greater than 1.5V voltage levels, which is more than adequate for a differential receiver to acknowledge a logic state. The 54 ohms is the equivalent of two 120 ohm termination resistors placed on each side of the transmission line and the input impedance of 256 receivers on the line.

The ZT485H transmitter has an enable control line which is active HIGH. A logic HIGH on DE (pin 3) will enable the differential outputs. A logic LOW on DE (pin 3) will disable the transmitter outputs. While disabled, the transmitter outputs are in high impedance.

RS-485 Receivers

Each transceiver contains one differential receiver that has an input sensitivity of 200mV. The input impedance of the receivers is typically 96K ohms. A wide common mode range of -7V to +12V allows for large ground potential differences between systems.

The ZT483H, ZT485H, ZT489H, and ZT491H receivers have an enable control input. A logic LOW on $\overline{RE}$ will enable the receiver, a logic HIGH on $\overline{RE}$ will disable the receiver. The receivers are equipped with the true fail-safe feature, which guarantees that the receiver output to be in a HIGH state when the input is left unconnected. When the receiver inputs are either open or short circuit, the receiver output will be in a HIGH state when $\overline{RE}$ enable is LOW.

The ZT485H, ZT490H, and ZT491H transmits and receives at data rates up to 10Mbps. The ZT483H, ZT488H, and ZT489H operates with data rates up to 250Kbps.

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Bus Configuration

The ZT488H, ZT489H, ZT490H, and ZT491H are full-duplex transceivers, while the ZT483H and ZT485H are half-duplex.

For full duplex, the devices are used as a four-wire bus transceiver with a configuration that the transmitters and receivers are moving data independent of each other. Transmit can occur on a dedicated two-wire pair and receive can occur on an adjacent two-wire pair, with each pair transferring data at up to 10Mbps (up to 250Kbps for the ZT488H and ZT489H).

Half duplex is a configuration where the transmitter outputs are connected to its receiver inputs. This application is common for two-wire interfaces where either the transmitter is active or the receiver is active. It is common to connect the enable inputs for the transmitter and receiver together so that a logic HIGH will enable the transmitter and disable the receiver. Conversely, a logic LOW will disable the transmitter and enable the transmitter. Half-duplex configurations and these devices are designed for bidirectional data transmission on multipoint twisted-pair cables for applications, such as digital motor controllers, remote sensors and terminals, industrial process control, security stations and environmental control systems.

ESD Immunity

Electro-Static Discharge (ESD) is an important factor when implementing a serial port into a system, especially in harsh environmental conditions. These industrial strength devices provide extra protection against ESD and are intended for harsh environments where high-speed data communication is important.

All of the ZT485H family of transceivers incorporates internal protection structures on all pins to protect against ESD charges encountered during handling and assembly. The driver outputs and receiver inputs have extra protection against static electricity as they are directly interfacing to the outside environment. As such, these pins against ESD of ±15KV without damage in all states of the transceiver's operation in the static state. After multiple ESD events, ASIX's ZT485H family of transceivers keep working without latchup. These devices eliminate the need for external transient suppressor diodes and the associated high capacitance loading, allowing reliable high-speed data communications.

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This test is intended to simulate the human body's potential to store electrostatic energy and discharge it to an integrated circuit upon close proximity or contact. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

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6 Function Table

ZT483H/ZT485H

DRIVER				RECEIVER		
Input	Enable	Outputs		Differential Inputs	Enable	Output
DI	DE	A	B	$V_{ID} = V_A - V_B$	$\overline{RE}$	RO
H	H	H	L	$V_{ID} \leq -0.2V$	L	L
L	H	L	H	$-0.2V < V_{ID} < +0.2V$	L	U
X	L	Z	Z	$+0.2V \leq V_{ID}$	L	H
Open	H	H	L	X	H	Z
X	Open	Z	Z	Open circuit	L	H*
				Short circuit	L	H*
				X	Open	Z

ZT488H/ZT490H

DRIVER			RECEIVER	
Input	Outputs		Differential Inputs	Output
DI	Y	Z	$V_{ID} = V_A - V_B$	RO
H	H	L	$V_{ID} \leq -0.2V$	L
L	L	H	$-0.2V < V_{ID} < +0.2V$	U
Open	H	L	$+0.2V \leq V_{ID}$	H
			Open circuit	H*
			Short circuit	H*

ZT489H/ZT491H

DRIVER				RECEIVER		
Input	Enable	Outputs		Differential Inputs	Enable	Output
DI	DE	Y	Z	$V_{ID} = V_A - V_B$	$\overline{RE}$	RO
H	H	H	L	$V_{ID} \leq -0.2V$	L	L
L	H	L	H	$-0.2V < V_{ID} < +0.2V$	L	U
X	L	Z	Z	$+0.2V \leq V_{ID}$	L	H
Open	H	H	L	X	H	Z
X	Open	Z	Z	X	Open	Z
				Open circuit	L	H*
				Short circuit	L	H*

Note:
H = High Level; L = Low Level; Z = High Impedance; X = Irrelevant; U = Undetermined State.
* = Fail Safe (Receiver Output High) when Receiver Inputs are Open or Short and Common Mode equals to 0V.

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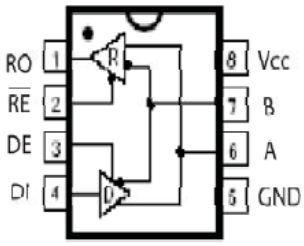
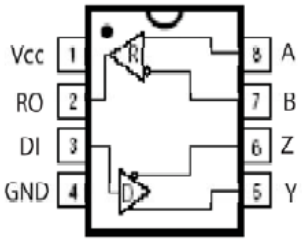
7 Pin Configuration

ZT483H/ZT485H



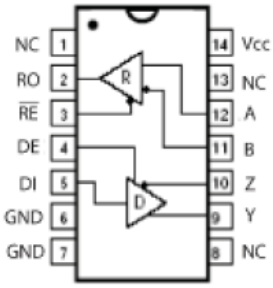
8-Pin PDIP/nSOIC

ZT488H/ZT490H



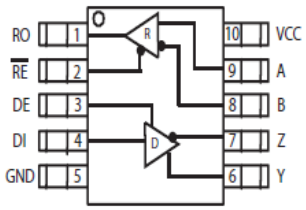
8-Pin PDIP/nSOIC

ZT489H/ZT491H



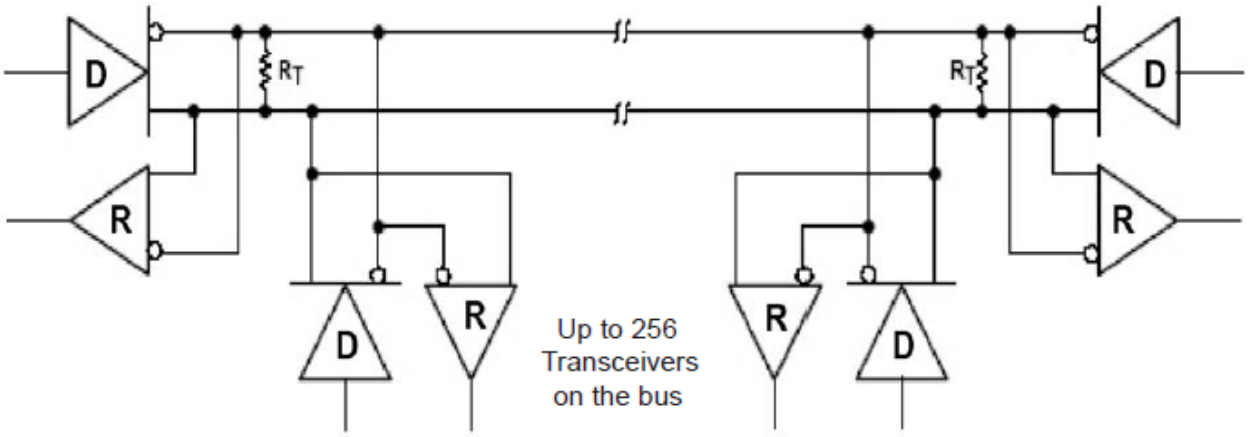
14-Pin PDIP/nSOIC

ZT491HLEEU



10-Pin MSOP

8 Typical Application Circuits



Notes:
A. The bus should be terminated at both ends in its characteristic impedance of $R_T = Z_O$.
B. Stub lengths off the main bus should be kept as short as possible.
C. Can connect up to 256 devices on the same common bus.

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9 Typical Test Circuits

Notes:
A. The test load capacitance includes probe and test jig capacitance, unless otherwise specified.
B. The signal generator had the following characteristics:
Pulse rate = 1000 KHz, 50% duty cycle, Z_O = 50Ω , t_r & t_f < 6ns, unless otherwise specified.

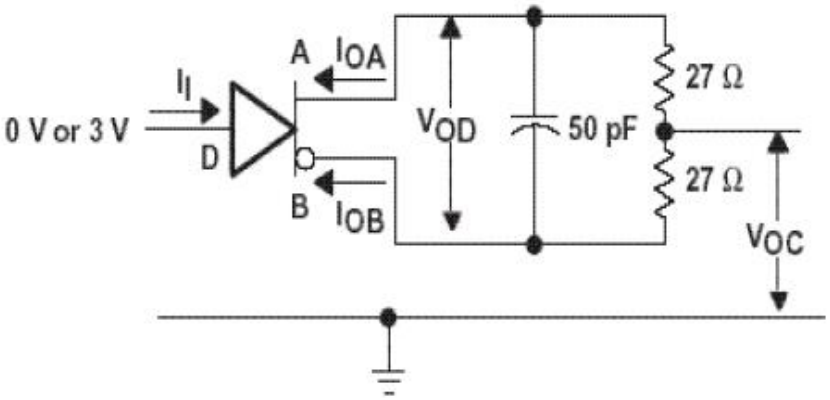

Figure 1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

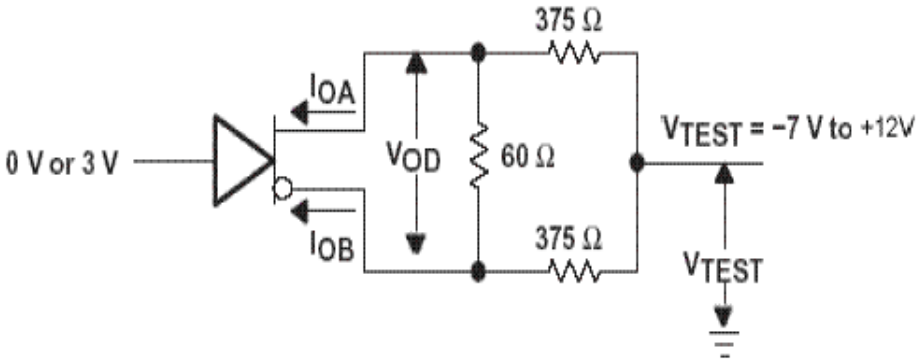

Figure 2. Driver Test Circuit, V_{OD} With Common-Mode Loading

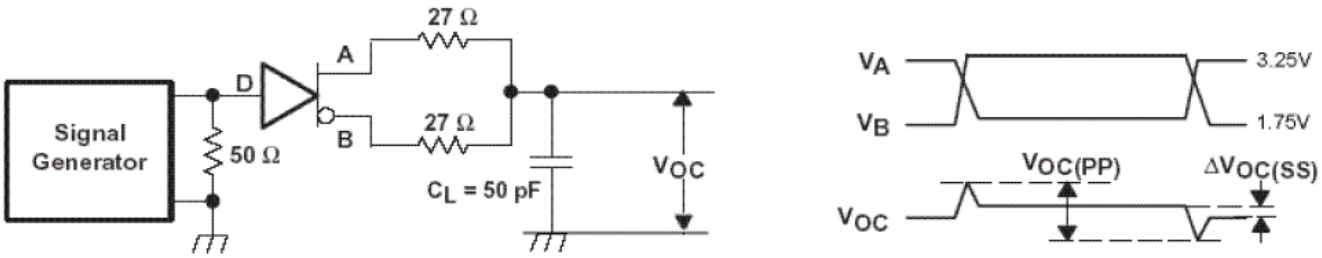

Figure 3. Driver Common-Mode Output Voltage (V_{OC}) Test Circuit and Waveforms

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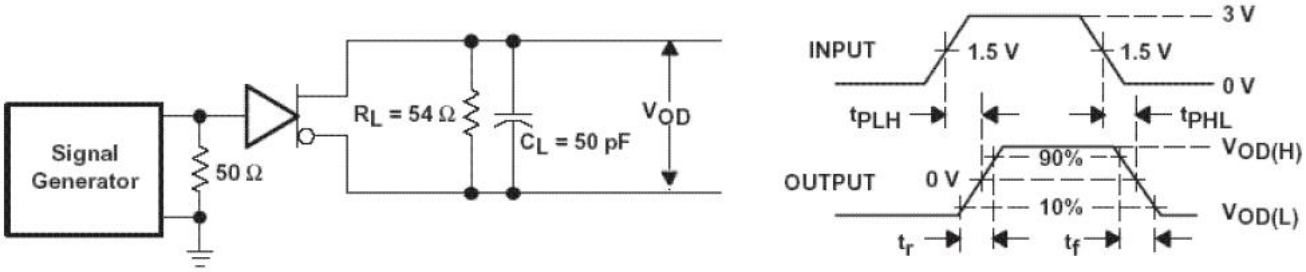

Figure 4. Driver Differential Output Voltage (V_{OD}) Switching Test Circuit and Waveforms

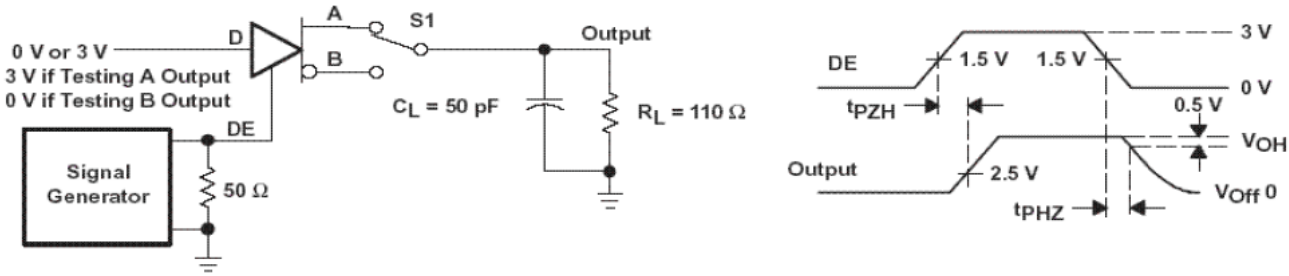

Figure 5. Driver Enable/Disable Test Circuit and Waveforms, High Output

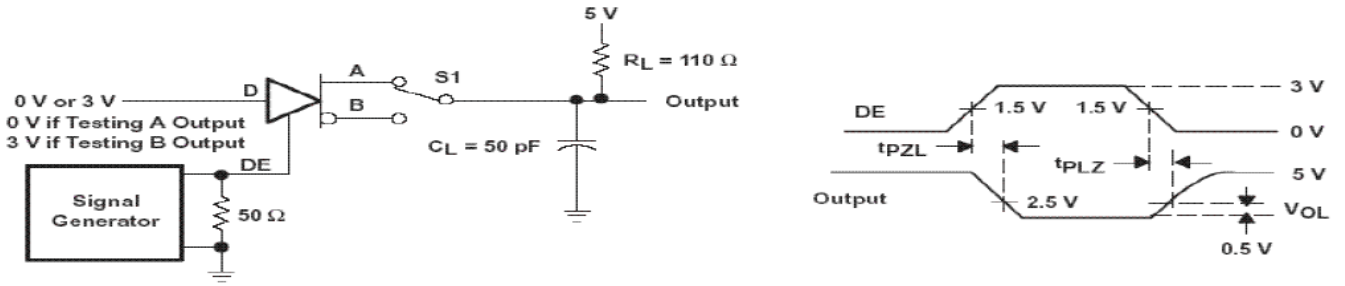

Figure 6. Driver Enable/Disable Test Circuit and Waveforms, Low Output

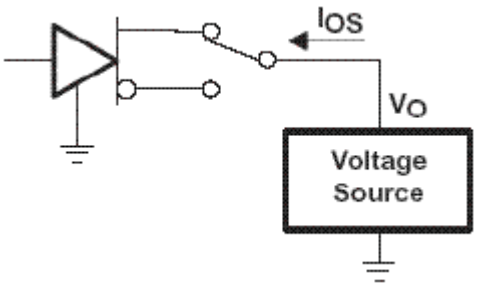

Figure 7. Driver Short-Circuit Test Configuration

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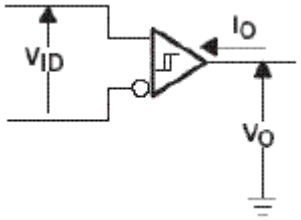

Figure 8. Receiver Parameter Definitions

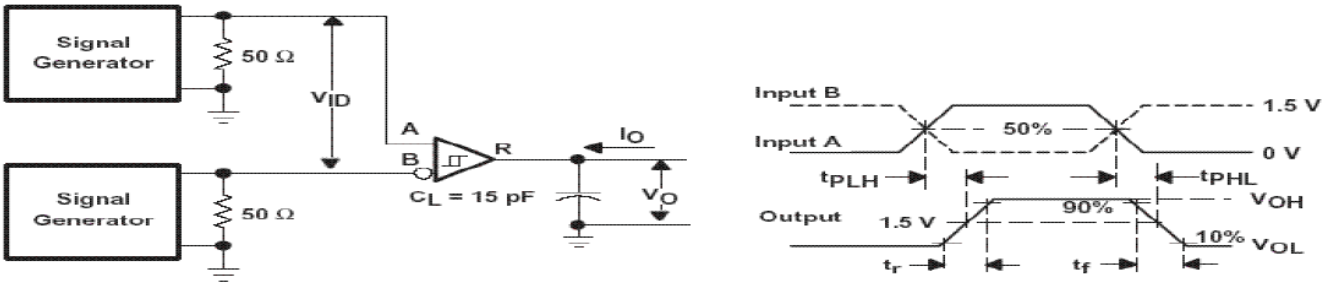

Figure 9. Receiver Propagation (t_{PLH} and t_{PHL})Test Circuit and Waveforms

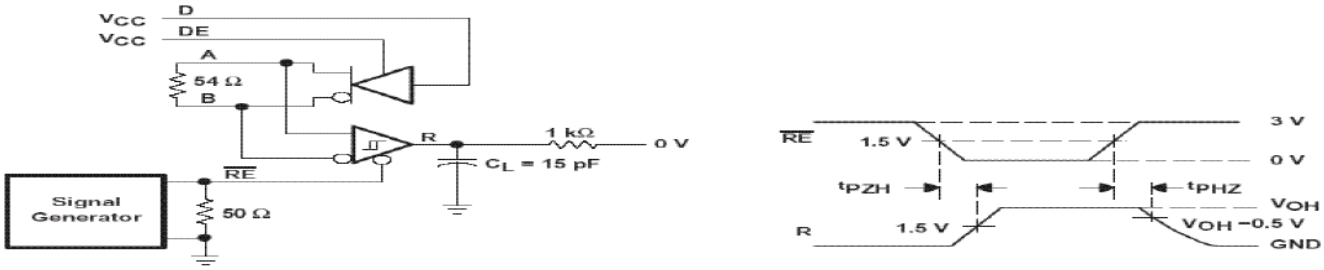

Figure 10. Receiver Output Enable/Disable Test Circuit and Waveforms, Data Output High

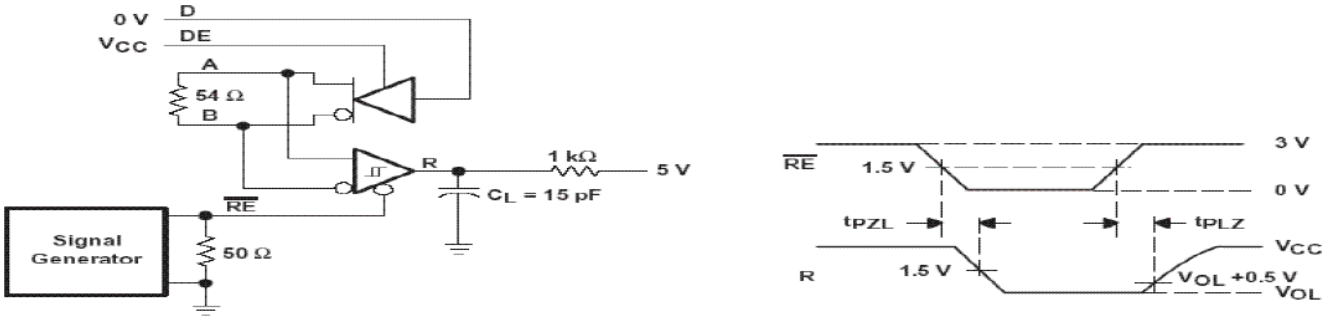

Figure 11. Receiver Output Enable/Disable Test Circuit and Waveforms, Data Output Low

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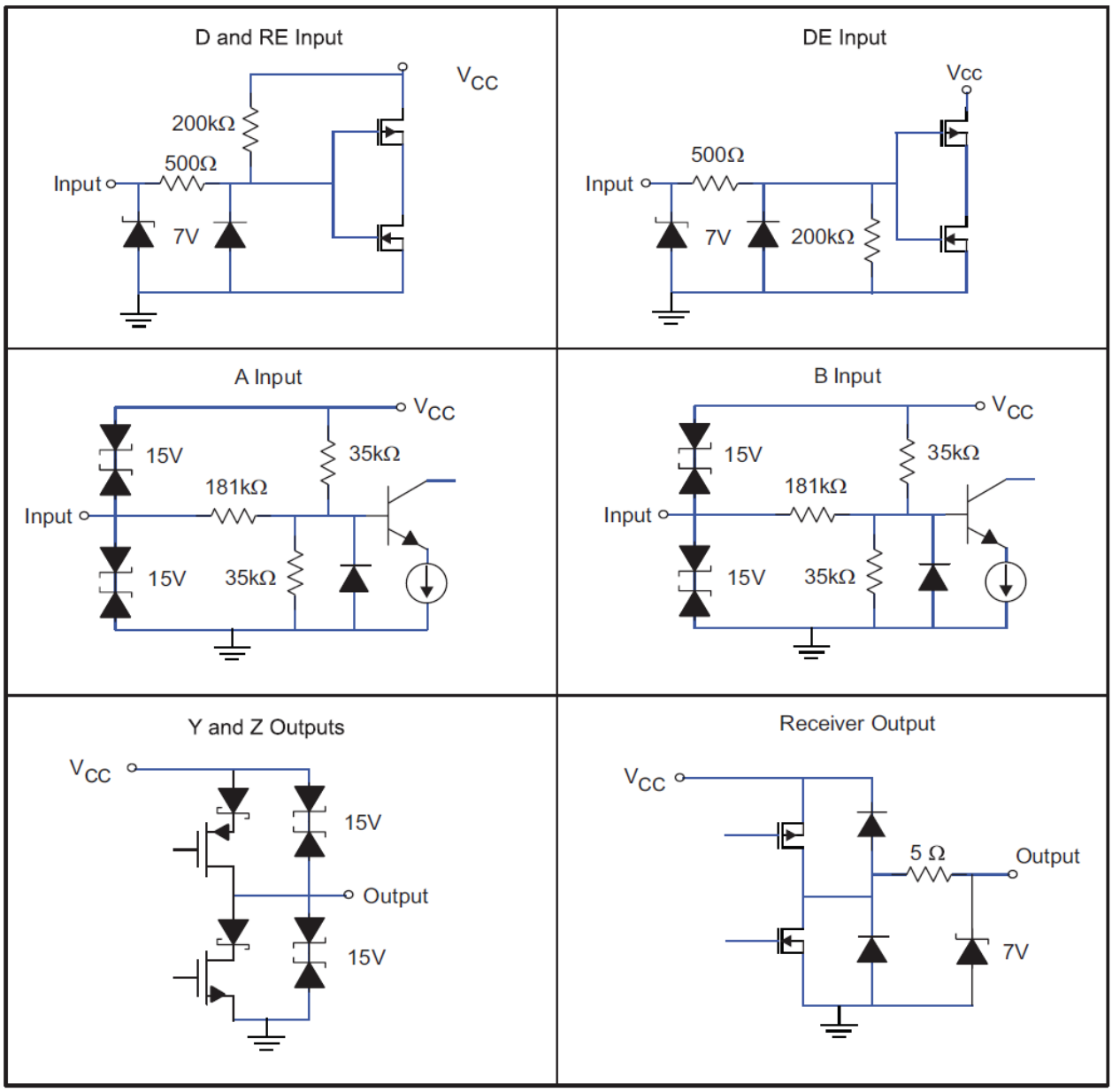
10 Equivalent Input and Output Schematic Diagrams



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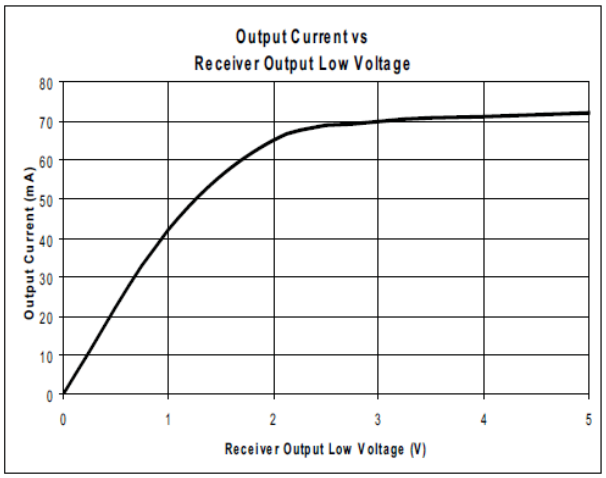
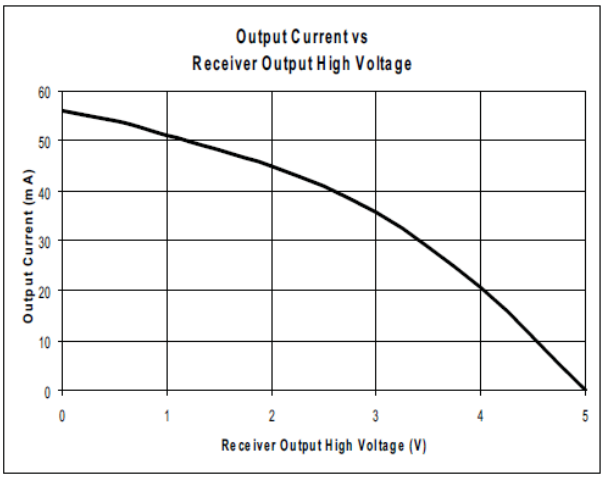
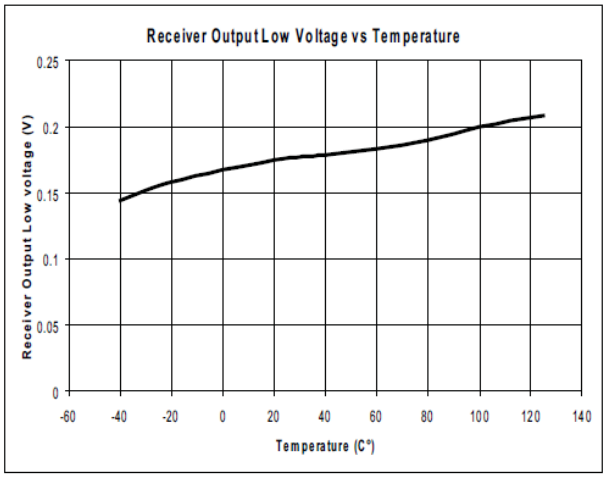
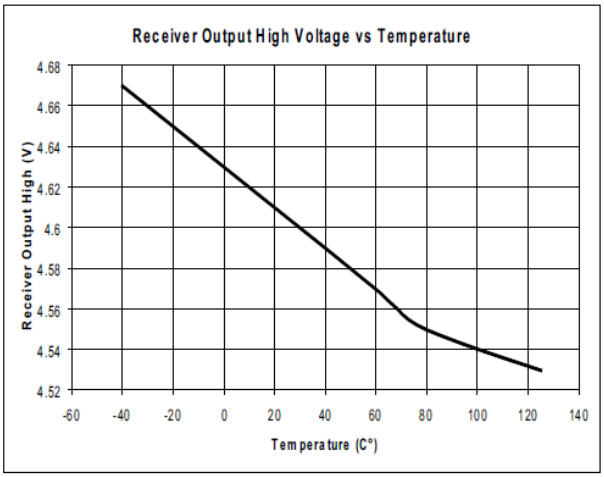
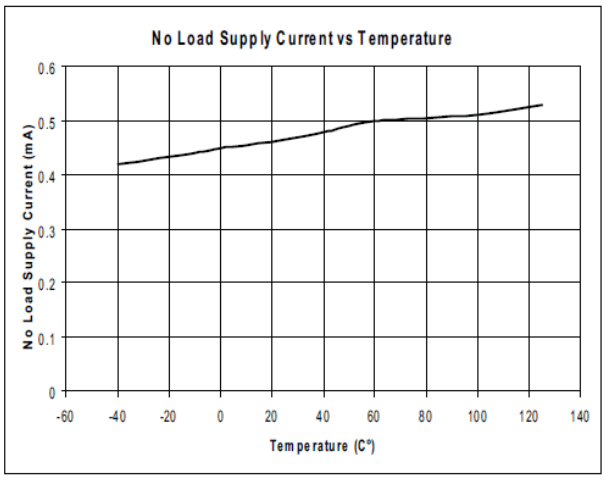
11 Typical Performance Characteristics

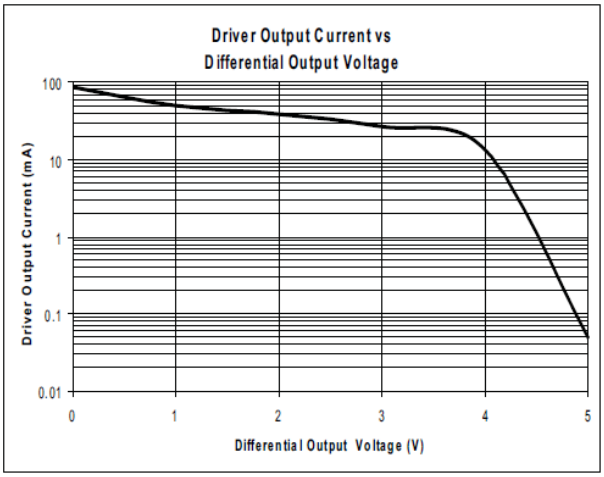












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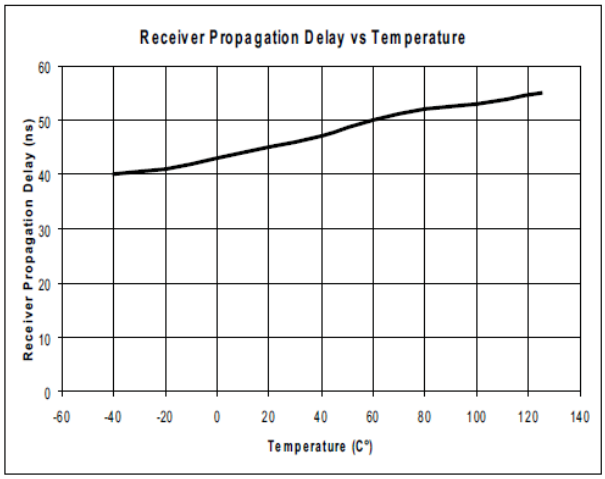

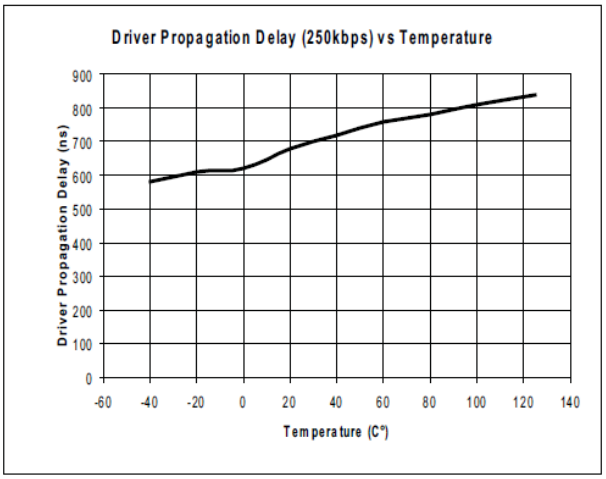

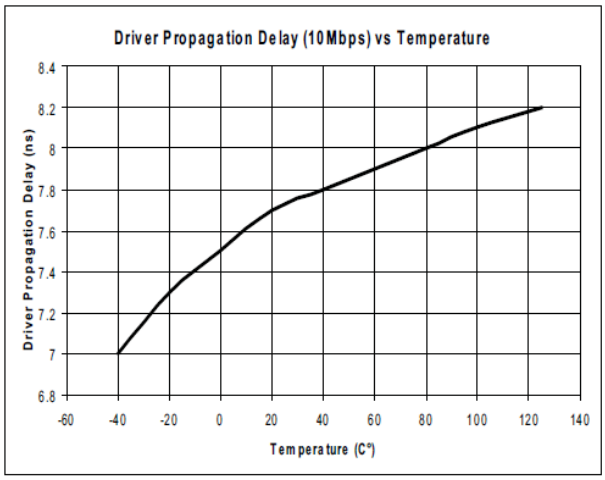

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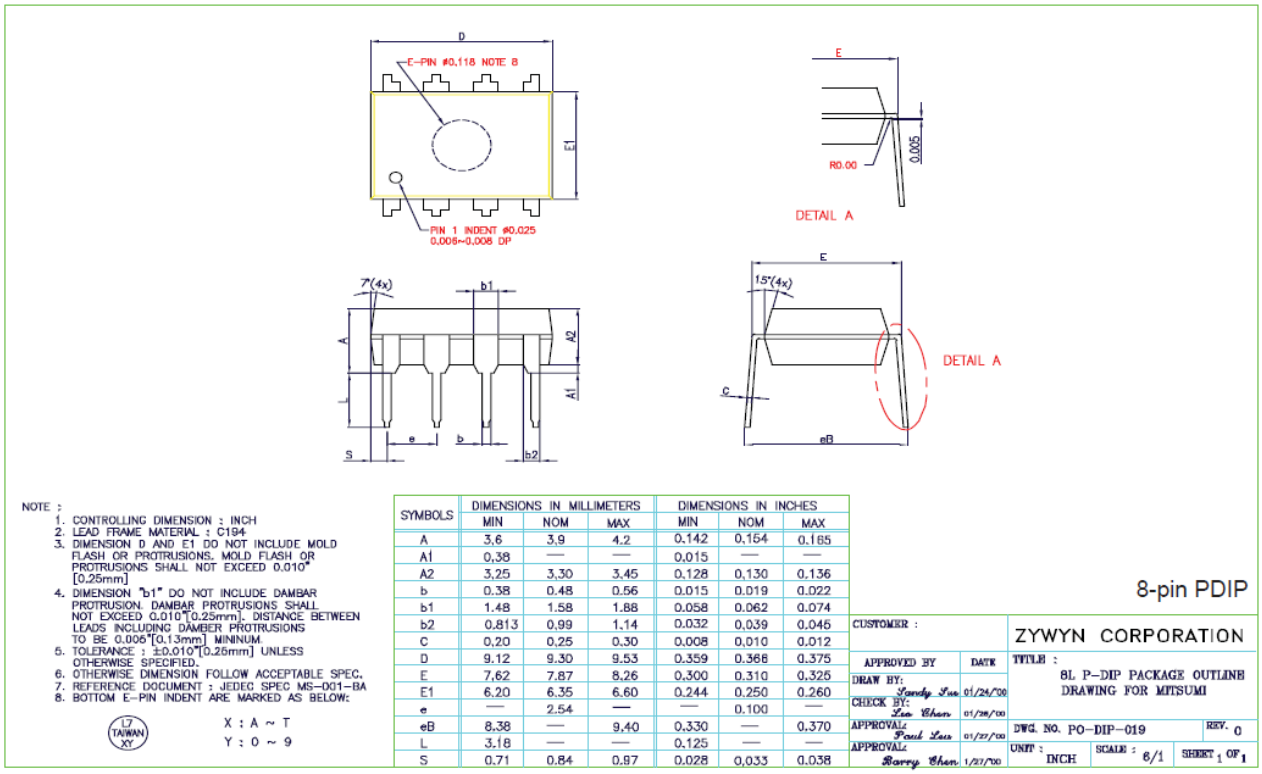
12 Package Information



NOTE :
1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : C194
3. DIMENSION D AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010" [0.25mm]
4. DIMENSION "b1" DO NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSIONS SHALL NOT EXCEED 0.010"[0.25mm]. DISTANCE BETWEEN LEADS INCLUDING DAMBER PROTRUSIONS TO BE 0.005"[0.13mm] MINIMUM.
5. TOLERANCE : ±0.010"[0.26mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-001-BA
8. BOTTOM E-PIN INDENT ARE MARKED AS BELOW:

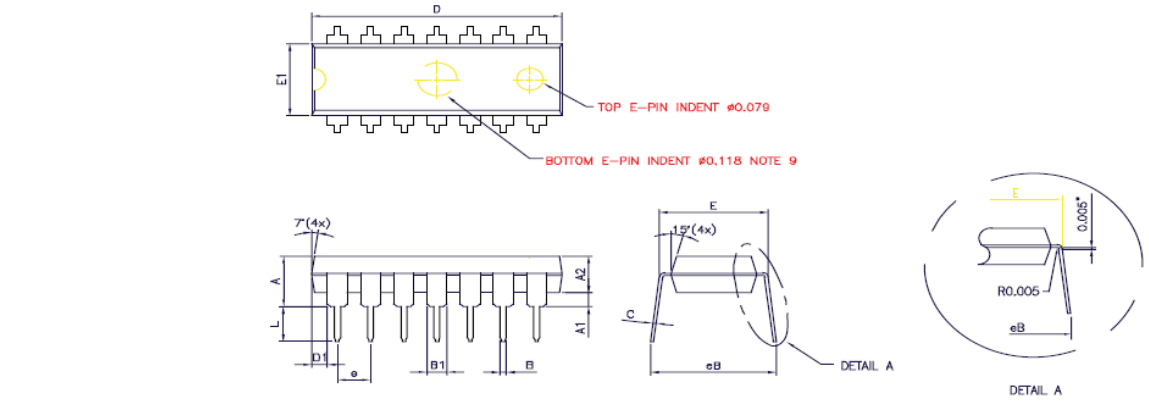
L7 TAIWAN XY

X : A ~ T
Y : 0 ~ 9

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.6	3.9	4.2	0.142	0.154	0.165
A1	0.38	—	—	0.015	—	—
A2	3.25	3.30	3.45	0.128	0.130	0.136
b	0.38	0.48	0.56	0.015	0.019	0.022
b1	1.48	1.58	1.88	0.058	0.062	0.074
b2	0.813	0.99	1.14	0.032	0.039	0.045
C	0.20	0.25	0.30	0.008	0.010	0.012
D	9.12	9.30	9.53	0.359	0.366	0.375
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.20	6.35	6.60	0.244	0.250	0.260
e	—	2.54	—	—	0.100	—
eB	8.38	—	9.40	0.330	—	0.370
L	3.18	—	—	0.125	—	—
S	0.71	0.84	0.97	0.028	0.033	0.038

8-pin PDIP

CUSTOMER :		ZYWYN CORPORATION
APPROVED BY	DATE	TITLE : 8L P-DIP PACKAGE OUTLINE DRAWING FOR MITSUMI
DRAW BY: Sandy Lee	01/24/'00	
CHECK BY: Leo Chen	01/28/'00	
APPROVAL: Paul Lee	01/27/'00	DWG. NO. PO-DIP-019 REV. 0
APPROVAL: Barry Chen	1/27/'00	UNIT : INCH SCALE : 8/1 SHEET 1 OF 1



NOTES :
1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL MATERIAL : C194
3. PACKAGE DIMENSION EXCLUDE MOLDING FLASH
4. AFTER SOLDER PLATING LEAD THICKNESS WILL BE 0.013" MAX
5. AFTER SOLDER DIPPING LEAD THICKNESS WILL BE 0.020" MAX
6. THE MAX. ALLOWABLE MOLDING FLASH IS 0.010"
7. TOLERANCE : 0.002" UNLESS OTHERWISE SPECIFIED
8. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPES
9. THE BOTTOM E- PIN INDENT IS MARKED AS BELOW :

TAIWAN XY

X : A-1
Y : 0-9

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	4.57	—	—	0.180
A1	0.38	—	—	0.015	—	—
A2	3.25	3.30	3.45	0.128	0.130	0.136
B	0.26	0.46	0.56	0.014	0.018	0.022
B1	1.14	1.27	1.52	0.045	0.050	0.060
C	0.20	0.25	0.33	0.008	0.010	0.013
D	18.19	19.15	19.30	0.744	0.754	0.760
D1	0.81	1.19	1.47	0.032	0.047	0.058
E	7.62	—	8.26	0.300	—	0.325
E1	6.35	6.50	6.65	0.250	0.256	0.262
e	—	2.54	—	—	0.100	—
L	3.18	—	—	0.125	—	—
eB	8.63	—	9.65	0.340	—	0.380

14-pin PDIP

CUSTOMER :		ZYWYN CORPORATION
APPROVED BY	DATE	TITLE : 14L P-DIP PACKAGE OUTLINE DRAWING
DRAW BY: Vent Chen	05/12/'00	
CHECK BY: Hamah Kao	5/12/'00	
APPROVAL: Paul Lee	5/12/'00	DWG. NO. PO-DIP-002 REV. 0
APPROVAL: Barry Chen	5/12/'00	UNIT : INCH SCALE : 4/1 SHEET 1 OF 1

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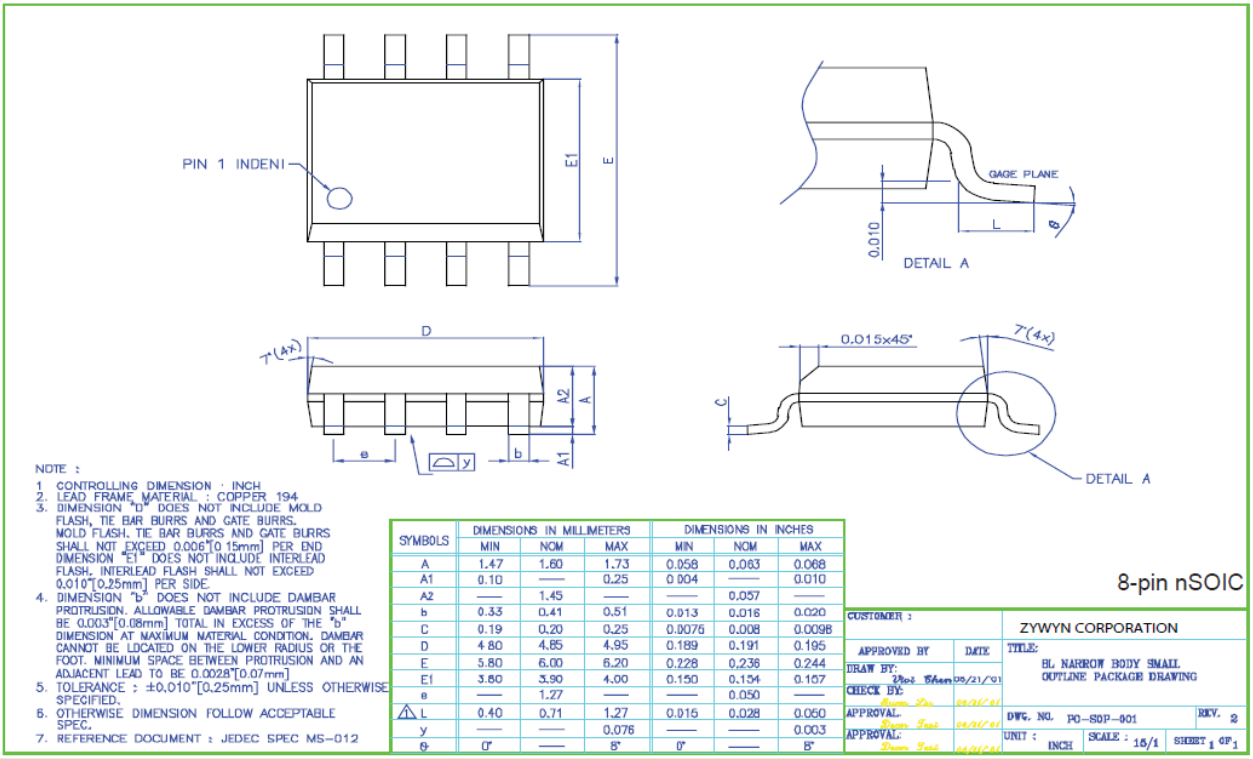
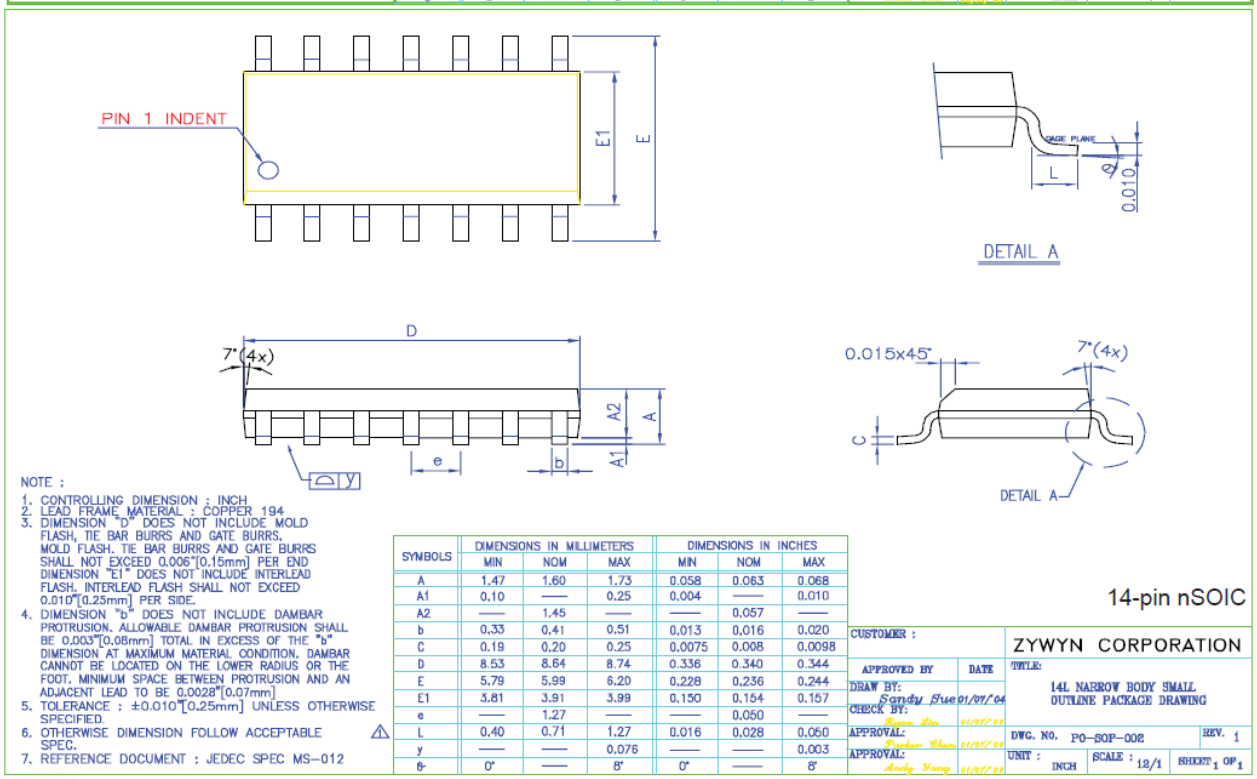


NOTE :
1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : COPPER 194
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH, INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-012

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.40	0.71	1.27	0.015	0.028	0.050
y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

8-pin nSOIC

CUSTOMER :		ZYWYN CORPORATION
APPROVED BY	DATE	TITLE: 8L NARROW BODY SMALL OUTLINE PACKAGE DRAWING
DRAW BY: Sandy Sue	09/21/'01	
CHECK BY: Ryan Yu	09/21/'01	
APPROVAL: Ryan Yu	09/21/'01	DWG. NO. PO-SOP-001 REV. 2
APPROVAL: Ryan Yu	09/21/'01	UNIT : INCH SCALE : 15/1 SHEET 1 OF 1



NOTE :
1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : COPPER 194
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH, INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-012

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	8.53	8.64	8.74	0.336	0.340	0.344
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.40	0.71	1.27	0.016	0.028	0.050
y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

14-pin nSOIC

CUSTOMER :		ZYWYN CORPORATION
APPROVED BY	DATE	TITLE: 14L NARROW BODY SMALL OUTLINE PACKAGE DRAWING
DRAW BY: Sandy Sue	01/07/'04	
CHECK BY: Ryan Yu	01/07/'04	
APPROVAL: Jordan Chen	01/07/'04	DWG. NO. PO-SOP-002 REV. 1
APPROVAL: Andy Yang	01/07/'04	UNIT : INCH SCALE : 12/1 SHEET 1 OF 1

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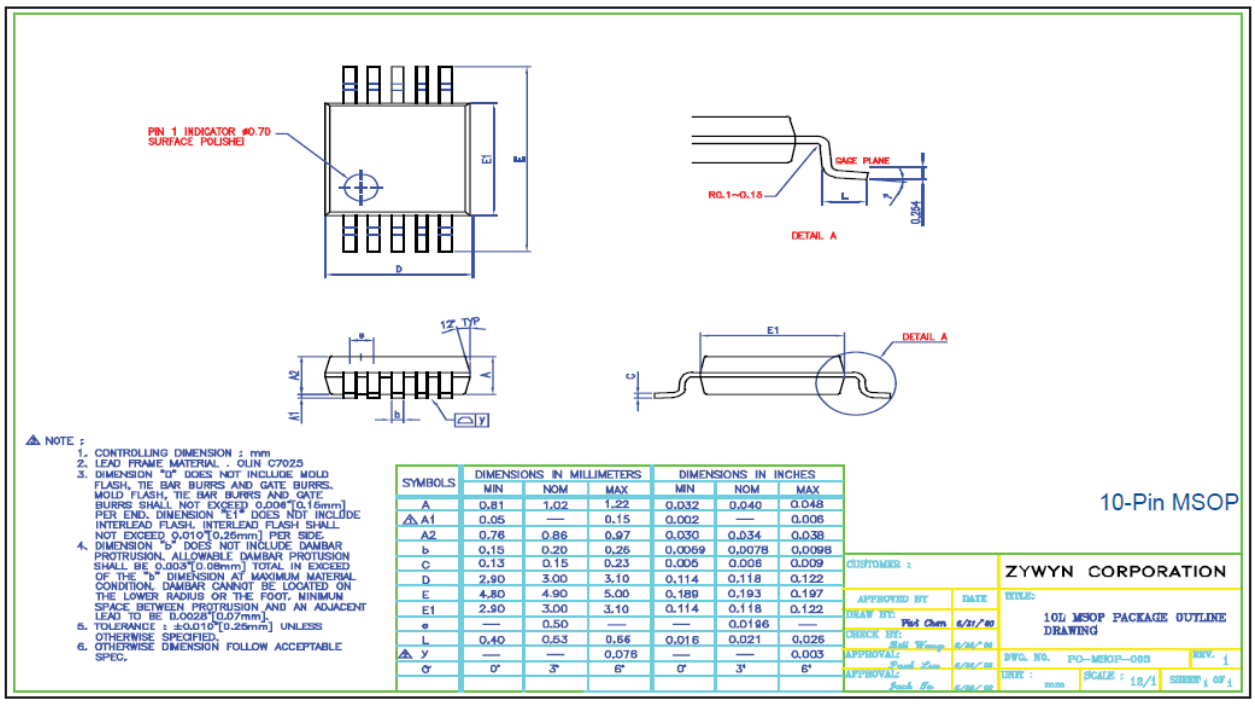

⚠ NOTE :
1. CONTROLLING DIMENSION : mm
2. LEAD FRAME MATERIAL : OLIN C7025
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCEED OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUN SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm].
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.81	1.02	1.22	0.032	0.040	0.048
⚠ A1	0.05	—	0.15	0.002	—	0.006
A2	0.76	0.86	0.97	0.030	0.034	0.038
b	0.15	0.20	0.25	0.0059	0.0078	0.0098
C	0.13	0.15	0.23	0.005	0.006	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.80	4.90	5.00	0.189	0.193	0.197
E1	2.90	3.00	3.10	0.114	0.118	0.122
e	—	0.50	—	—	0.0196	—
L	0.40	0.53	0.66	0.016	0.021	0.026
⚠ y	—	—	0.076	—	—	0.003
θ	0°	3°	6°	0°	3°	6°

10-Pin MSOP

CUSTOMER :		ZYWYN CORPORATION
APPROVED BY	DATE	TITLE: 10L MSOP PACKAGE OUTLINE DRAWING
DRAW BY: Pei Chen	6/21/'00	
CHECK BY: Bill Wang	6/26/'00	
APPROVAL: Frank Yan	6/26/'00	DWG. NO. PO-MSOP-003 REV. 1
APPROVAL: Jack Fu	6/26/'00	UNIT : mm SCALE : 12/1 SHEET 1 OF 1

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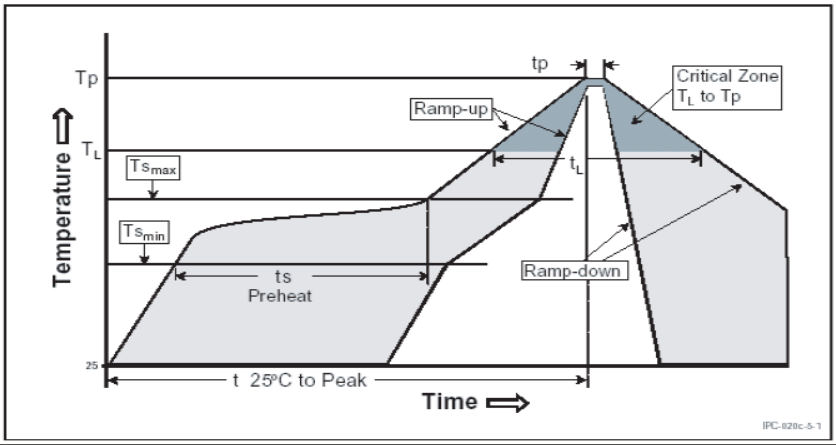
13 Green Package SMD IR Reflow Prof le Information

IR Reflow Profile Conditions		
Profile Feature	**JESD Sn-Pb Eutectic Assembly**	**JESD Pb-free Assembly**
Average Ramp-Up Rate (T_{Smax} to T_P)	3°C/second max.	3°C/second max.
Pre-heat - Temperature Min (T_{Smin}) - Temperature Max (T_{Smax}) - Time (T_{Smin} to t_{Smax})	 100°C 150°C 60~120 seconds	 150°C 200°C 60~180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	 183°C 60~150 seconds	 217°C 60~150 seconds
Peak/Classification Temperature (T_P)	235°C+5/-0°C	255°C+5/-0°C
Time within 5°C of actual Peak Temperature (t_P)	10~30 seconds	20~40 seconds
Ramp-Down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

ASIX Green Packages are Pb-free and RoHS compliance.

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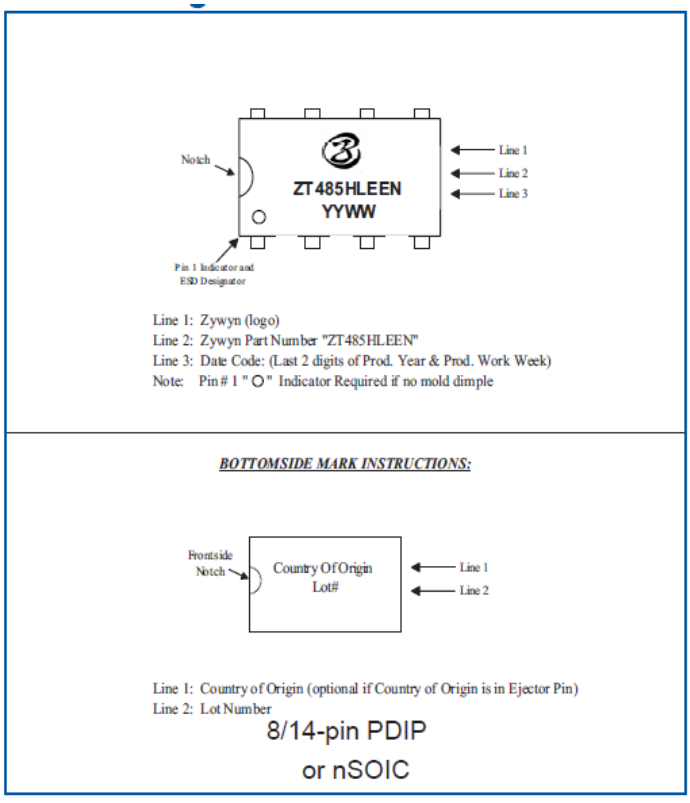
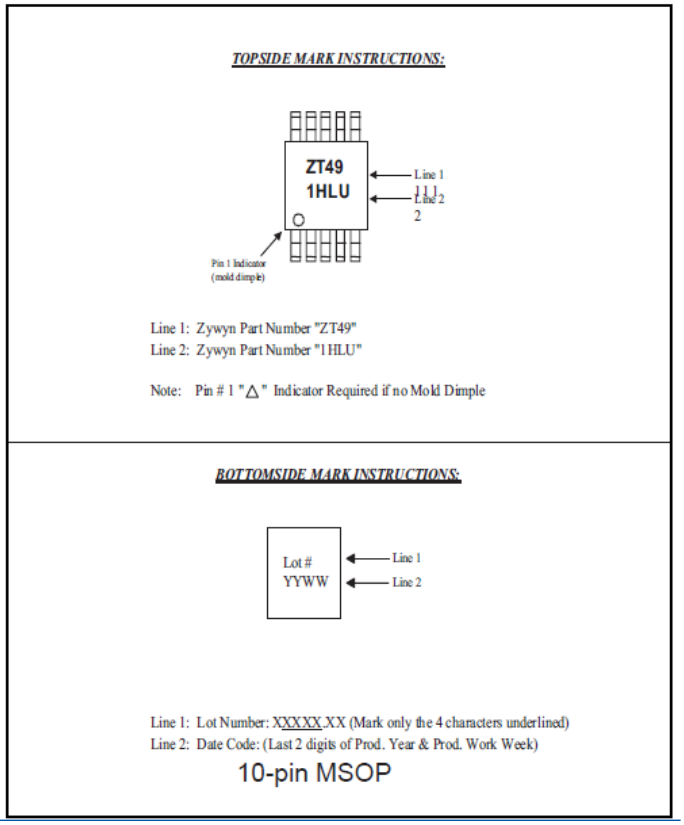
14 Ordering Information

Part Number	Temperature Range	Package Type	Green Package	MOQ/Tube	MOQ/T&R
ZT483HLEEN	-40°C to +85°C	8-pin nSOIC	✓	100	2500
ZT483HLEEP	-40°C to +85°C	8-pin PDIP	✓	60	N/A
ZT485HLEEN	-40°C to +85°C	8-pin nSOIC	✓	100	2500
ZT485HLEEP	-40°C to +85°C	8-pin PDIP	✓	60	N/A
ZT488HLEEN	-40°C to +85°C	8-pin nSOIC	✓	100	2500
ZT488HLEEP	-40°C to +85°C	8-pin PDIP	✓	60	N/A
ZT489HLEEN	-40°C to +85°C	14-pin nSOIC	✓	58	2500
ZT489HLEEP	-40°C to +85°C	14-pin PDIP	✓	30	N/A
ZT490HLEEN	-40°C to +85°C	8-pin nSOIC	✓	100	2500
ZT490HLEEP	-40°C to +85°C	8-pin PDIP	✓	60	N/A
ZT491HLEEN	-40°C to +85°C	14-pin nSOIC	✓	58	2500
ZT491HLEEP	-40°C to +85°C	14-pin PDIP	✓	30	N/A
ZT491HLEEU	-40°C to +85°C	10-pin MSOP	✓	50	2500

Please contact the factory for pricing, availability on Tape-and-Reel and Die Sales options.

15 Part Marking Information





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Revision History

Revision	Date	Comment
V1.6	2012/06/01	Initial release to customers
V2.00	2015/04/08	1. Changed to ASIX Electronics Corp. logo, strings and contact information. 2. Added ASIX copyright legal header information. 3. Modified the Revision History table format.
V2.10	2015/05/13	1. Modified some information in Feature, Section 1 and 9.

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